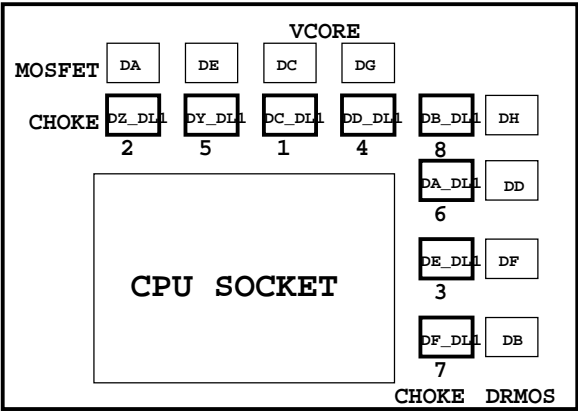


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCH HDMI/DP
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*8 SLOT
17	PCI EXPRESS*16/*8 SWITCH
18	PCI EXPRESS*1 SLOTS X3
19	PCI EXPRESS*4 SLOT
20	Dual BIOS
21	ALC1150
22	REAR AUDIO JACK
23	IR3563A PWM
24	IR3550-VCORE
25	IR3570-DDR PWM
26	IR3598-DDR POWER
27	5VDUAL, 3VDAUL, ERP

28	PCH1.05V, PCH1.5V, VCC3_DAC
29	I/O ITE8620 CX LPC
30	USB3 KB/USB3
31	F_PANEL , F_USB , PHOT
32	F_USB 2.0& TPM
33	F_USB 3.0
34	ATX POWER, CLOCK GEN
35	HWM, FAN CTRL
36	INTEL I217
37	Marvell 9172
38	M.2 SATA EXTRESS
39	RST, PWR, CLR_CMOS
40-41	USB 3.0 uPD720201. POWER
42	M3 POWER
43	PLX8605
44	DP SW126
45-46	TBT-CIO.PWR
47-48	TBT-mDP1.TBT-mDP2
49	TABLE LIST

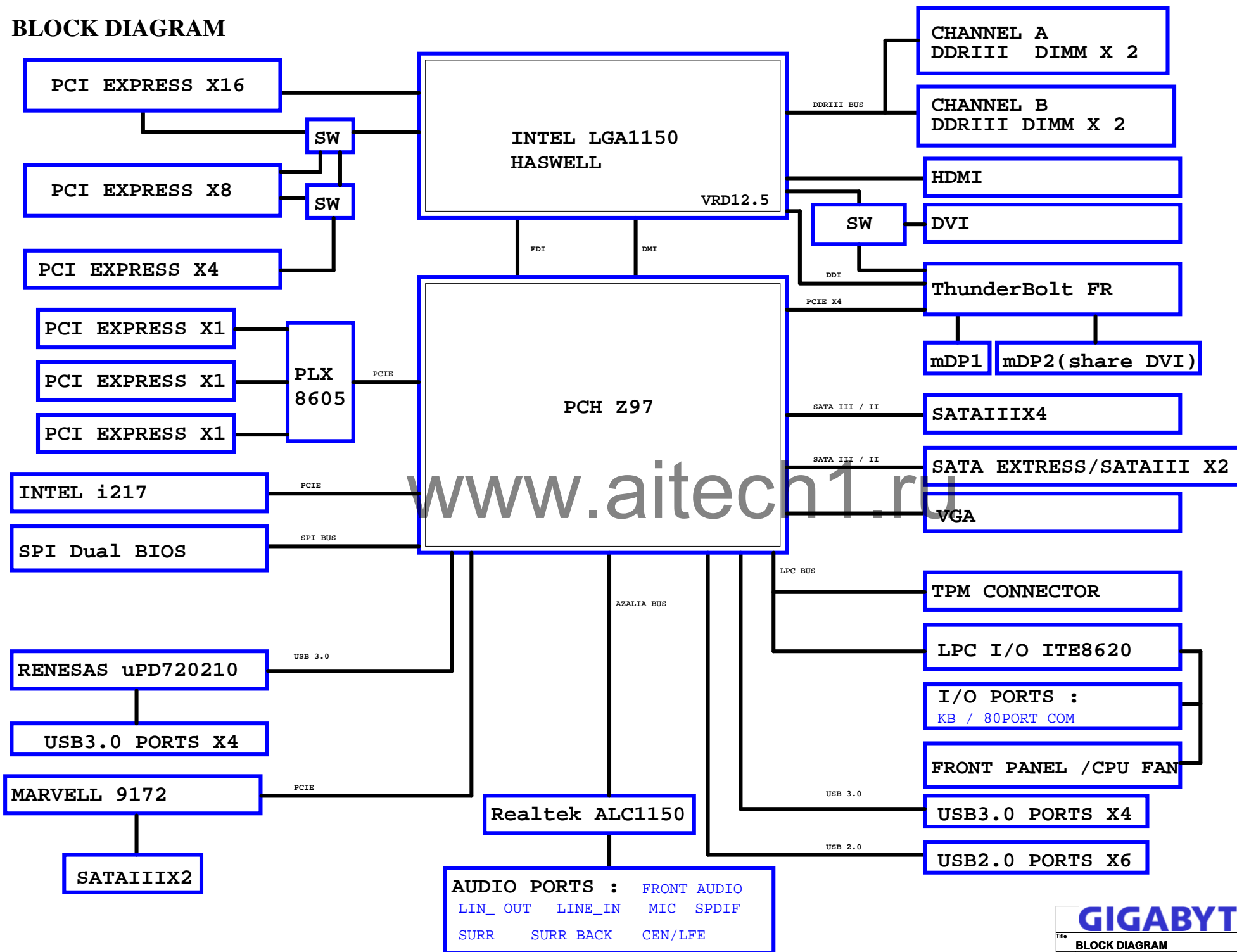


Component value change history

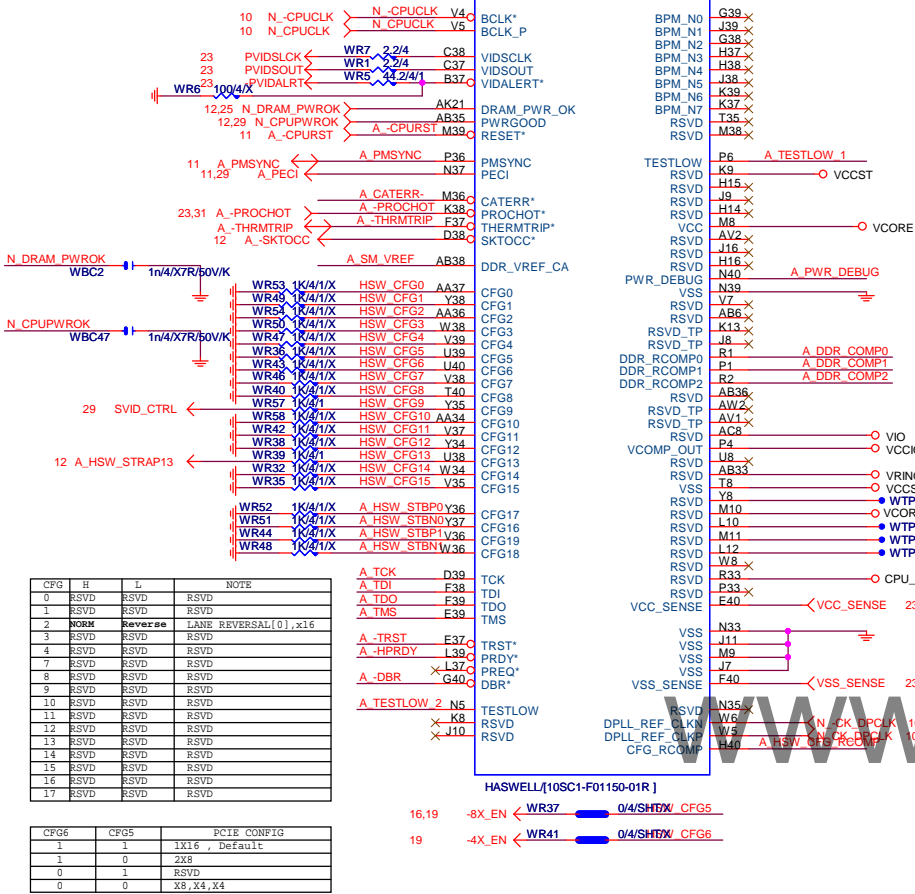
[illegible]

DATE	Change Item	Reason
2013/11/14	REV0.1 Z87X-UD3H 0.1 gerber out	
2014/03/28	REV1.0 1. 移除THR77 THR78(TBT) 2. 修改HD LED線路 3. BIOS LED燈號置中 4. BC6 BC7上移(避免HEATSINK導管撞到CHOKE) 5. AUDIO LED跟電組 MASK 5. 修改PXU1 FOOTPRINT(SIZE太大) 6. ADD THA_C22 THB_C22(TBT OVERSHOOT過高ISSUE預留)	

BLOCK DIAGRAM

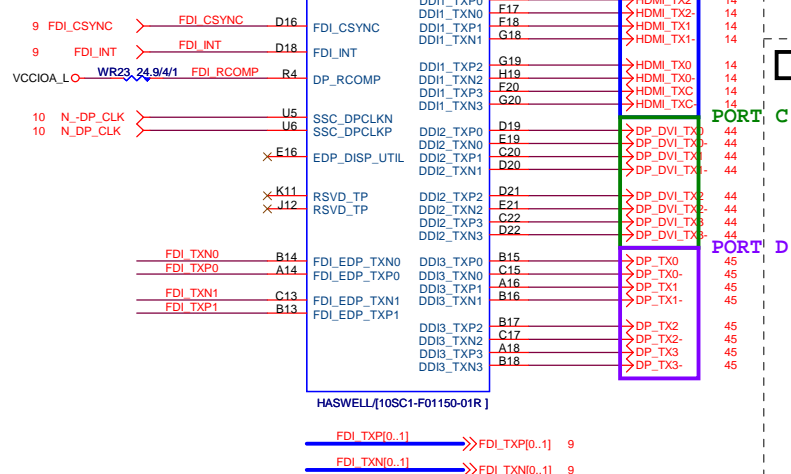


LGA1150 (E)



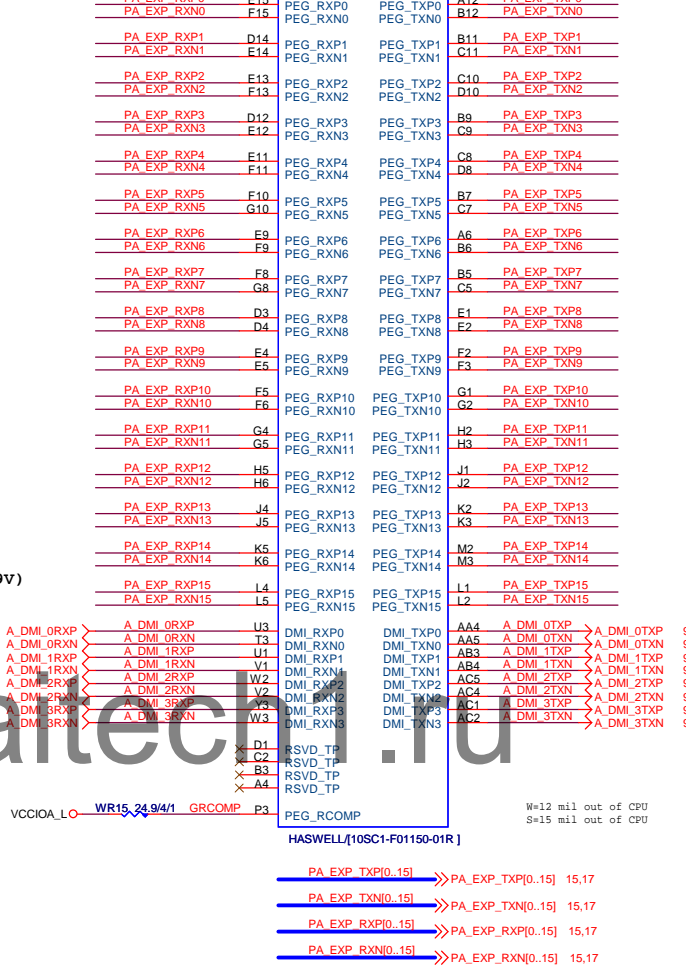
LGA1150

(D)

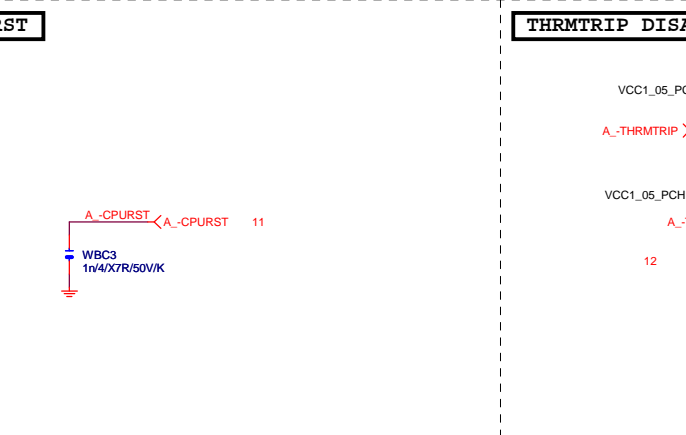


LGA1150

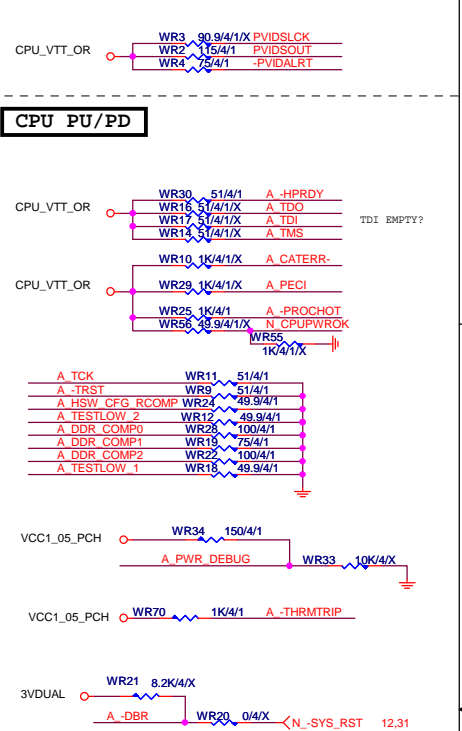
(C)



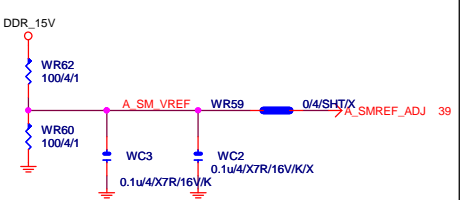
-CPURST



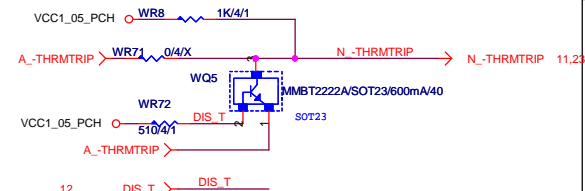
CPU SVID



SM REF



THRMTRIP DISABLE



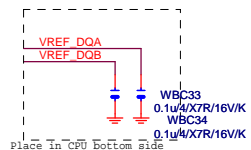
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MAAA4	AU17	DDR0_DQ4	AD37	MDA4
MAAA5	AW18	DDR0_DQ5	AD40	MDA5
MAAA6	AV17	DDR0_DQ6	AF37	MDA6
MAAA7	AT18	DDR0_DQ7	AF40	MDA7
MAAA8	AU18	DDR0_DQ8	AH40	MDA8
MAAA9	AT19	DDR0_DQ9	AH39	MDA9
MAAA10	AW11	DDR0_DQ10	AK38	MDA10
MAAA11	AV19	DDR0_DQ11	AK39	MDA11
MAAA12	AU19	DDR0_DQ12	AH37	MDA12
MAAA13	AY10	DDR0_DQ13	AH38	MDA8
MAAA14	AT20	DDR0_DQ14	AK37	MDA14
MAAA15	AU21	DDR0_DQ15	AK40	MDA15
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MODT_A1	AY8	DDR0_DQ17	AM39	MDA21
MODT_A2	AW9	DDR0_DQ18	AP38	MDA18
MODT_A3	AU8	DDR0_DQ19	AP39	MDA19
		DDR0_DQ20	AM37	MDA20
		DDR0_DQ21	AM38	MDA16
		DDR0_DQ22	AP37	MDA23
		DDR0_DQ23	AP40	MDA25
		DDR0_DQ24	AW37	MDA29
		DDR0_DQ25	AU35	MDA26
		DDR0_DQ26	AV35	MDA27
		DDR0_DQ27	AT37	MDA28
		DDR0_DQ28	AU37	MDA24
		DDR0_DQ29	AT35	MDA30
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		DDR0_DQ38	AR1	MDA41
		DDR0_DQ39	AR4	MDA45
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		DDR0_DQ41	AN4	MDA43
		DDR0_DQ42	AR2	MDA44
		DDR0_DQ43	AR3	MDA40
		DDR0_DQ44	AN2	MDA46
		DDR0_DQ45	AN1	MDA47
		DDR0_DQ46	AL1	MDA49
		DDR0_DQ47	AL4	MDA53
		DDR0_DQ48	AJ3	MDA50
		DDR0_DQ49	AJ4	MDA51
		DDR0_DQ50	AJ2	MDA52
		DDR0_DQ51	AL3	MDA48
		DDR0_DQ52	AJ2	MDA54
		DDR0_DQ53	AJ1	MDA55
		DDR0_DQ54	AG4	MDA57
		DDR0_DQ55	AE3	MDA58
		DDR0_DQ56	AE4	MDA59
		DDR0_DQ57	AG2	MDA60
		DDR0_DQ58	AG3	MDA56
		DDR0_DQ59	AE1	MDA63
		DDR0_DQ60	AE39	DQSA0
		DDR0_DQ61	AJ39	DQSA1
		DDR0_DQ62	AN39	DQSA2
		DDR0_DQ63	AV36	DQSA3
		DDR0_DQ64	AV5	DQSA4
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		DDR0_DQ67	AF3	DQSA7
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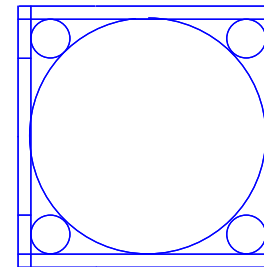
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LGA1150B

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MAAB3	AM23	DDR1_DQ3	AH35	MDB3
MAAB4	AP23	DDR1_DQ4	AD34	MDB4
MAAB5	AL23	DDR1_DQ5	AD35	MDB5
MAAB6	AY24	DDR1_DQ6	AG34	MDB6
MAAB7	AV25	DDR1_DQ7	AL34	MDB7
MAAB8	AU26	DDR1_DQ8	AL35	MDB8
MAAB9	AW25	DDR1_DQ9	AL35	MDB9
MAAB10	AP18	DDR1_DQ10	AK31	MDB10
MAAB11	AY25	DDR1_DQ11	AL31	MDB11
MAAB12	AV26	DDR1_DQ12	AK34	MDB12
MAAB13	AV27	DDR1_DQ13	AK35	MDB13
MAAB14	AV27	DDR1_DQ14	AK32	MDB14
MAAB15	AY28	DDR1_DQ15	AL32	MDB15
		DDR1_DQ16	AN34	MDB17
		DDR1_DQ17	AP34	MDB21
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		DDR1_DQ20	AN35	MDB20
		DDR1_DQ21	AP35	MDB16
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		DDR1_DQ23	AP32	MDB22
		DDR1_DQ24	AM29	MDB25
		DDR1_DQ25	AM28	MDB28
		DDR1_DQ26	AR29	MDB27
		DDR1_DQ27	AR28	MDB30
		DDR1_DQ28	AL29	MDB24
		DDR1_DQ29	AL28	MDB29
		DDR1_DQ30	AP29	MDB26
		DDR1_DQ31	AP28	MDB31
		DDR1_DQ32	AR12	MDB32
		DDR1_DQ33	AP12	MDB33
		DDR1_DQ34	AL13	MDB34
		DDR1_DQ35	AL12	MDB35
		DDR1_DQ36	AR13	MDB36
		DDR1_DQ37	AP13	MDB37
		DDR1_DQ38	AM13	MDB38
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		DDR1_DQ40	AR9	MDB45
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		DDR1_DQ42	AR6	MDB47
		DDR1_DQ43	AP6	MDB43
		DDR1_DQ44	AR10	MDB44
		DDR1_DQ45	AP10	MDB40
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		DDR1_DQ47	AP7	MDB42
		DDR1_DQ48	AM9	MDB52
		DDR1_DQ49	AL9	MDB53
		DDR1_DQ50	AL6	MDB50
		DDR1_DQ51	AL7	MDB55
		DDR1_DQ52	AL10	MDB49
		DDR1_DQ53	AM6	MDB54
		DDR1_DQ54	AM7	MDB51
		DDR1_DQ55	AH6	MDB61
		DDR1_DQ56	AH7	MDB60
		DDR1_DQ57	AE6	MDB59
		DDR1_DQ58	AE7	MDB63
		DDR1_DQ59	AJ6	MDB56
		DDR1_DQ60	AJ7	MDB57
		DDR1_DQ61	AE6	MDB58
		DDR1_DQ62	AE7	MDB62
		DDR1_DQ63	AE35	DQSB0
		DDR1_DQ64	AL33	DQSB1
		DDR1_DQ65	AN28	DQSB2
		DDR1_DQ66	AN28	DQSB3
		DDR1_DQ67	AN12	DQSB4
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		DDR1_DQ69	AL8	DQSB6
		DDR1_DQ70	AG7	DQSB7
		DDR1_DQ71	AN25	DQSB0
		DDR1_DQ72	AK33	DQSB1
		DDR1_DQ73	AN33	DQSB2
		DDR1_DQ74	AN29	DQSB3
		DDR1_DQ75	AN13	DQSB4
		DDR1_DQ76	AR8	DQSB5
		DDR1_DQ77	AM8	DQSB6
		DDR1_DQ78	AG6	DQSB7
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HASWELL[10SC1-F01150-01R]

CPU
ILM_BP/1156/CSP[12KRC-0F0001-61R]

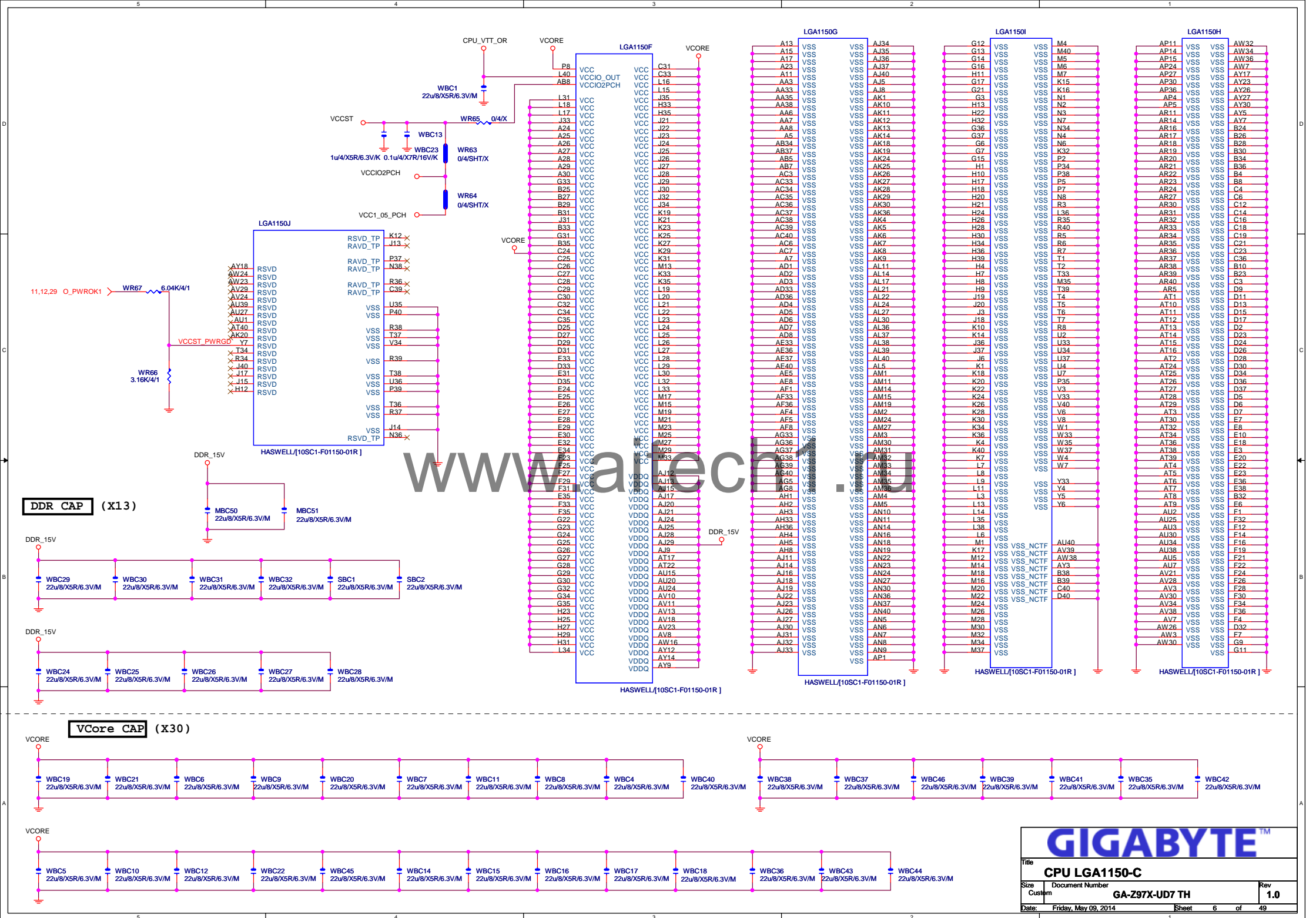
Need check the new CPU ME

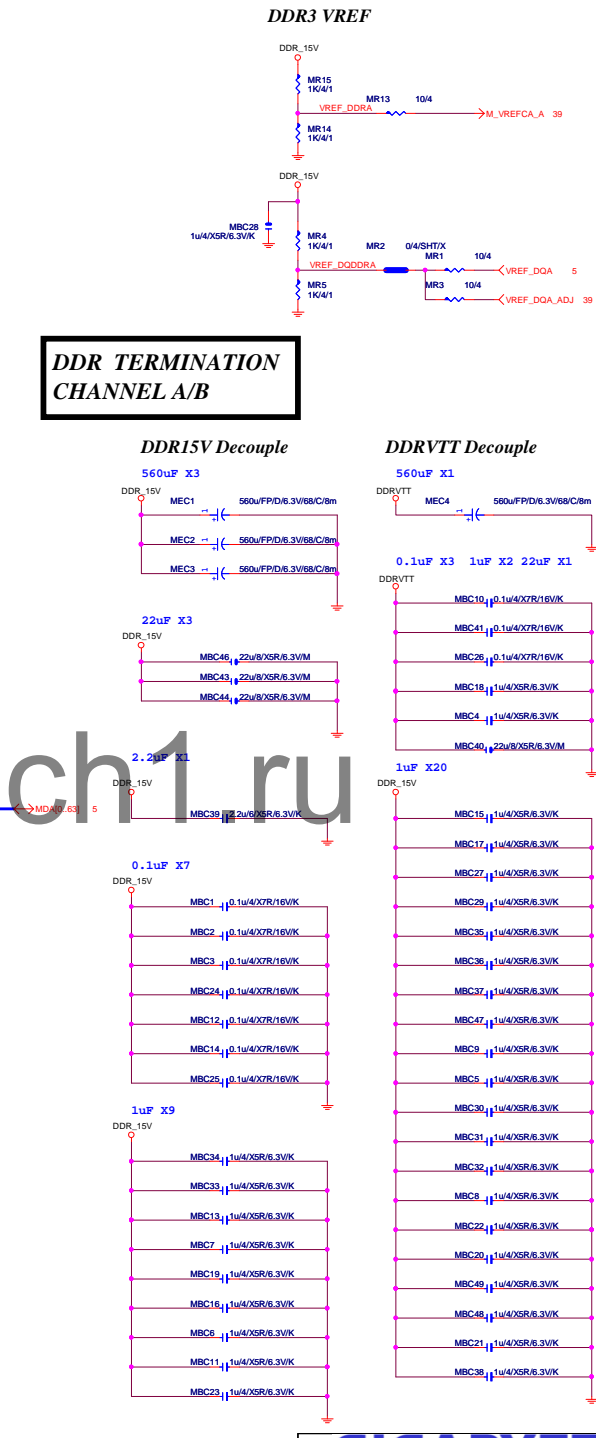
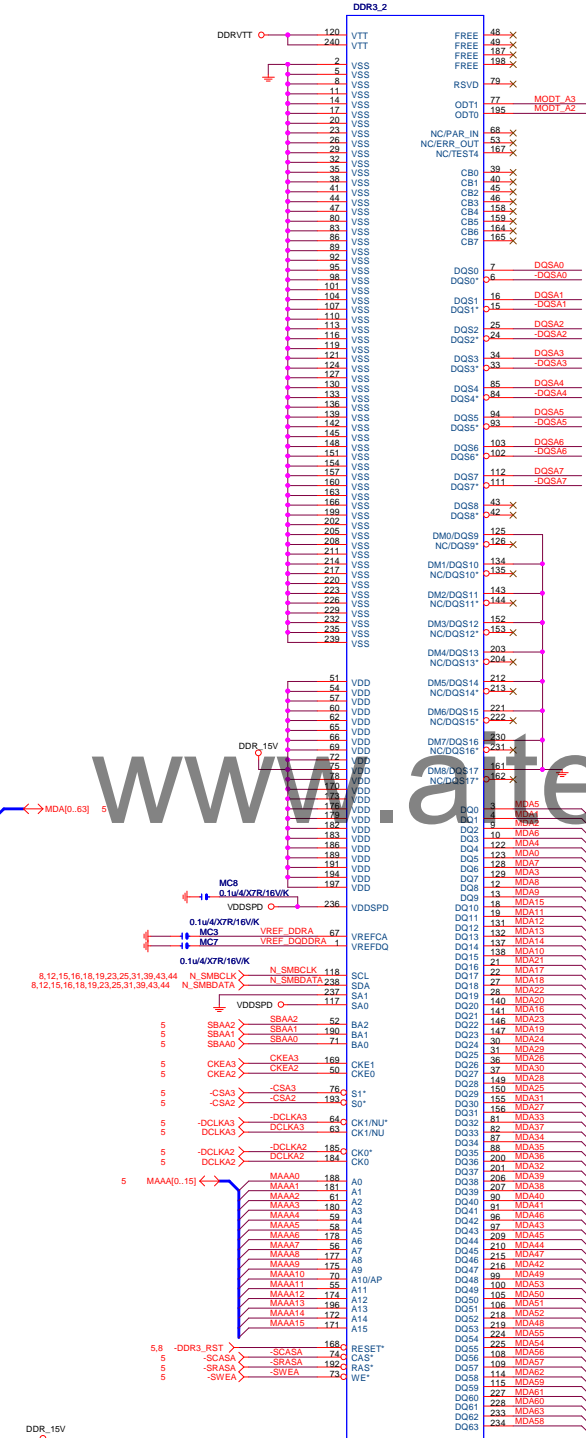
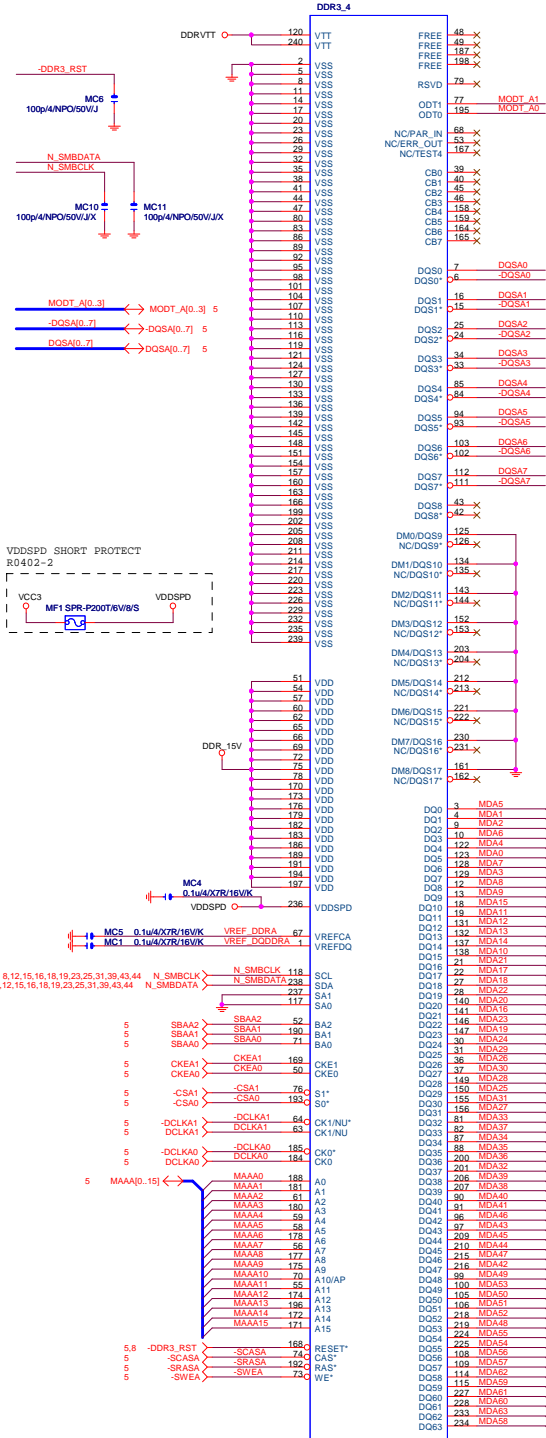
DDR BUS

7	MODT_A[0..3]	MODT_A[0..3]
8	MODT_B[0..3]	MODT_B[0..3]
7	MDA[0..63]	MDA[0..63]
8	MDB[0..63]	MDB[0..63]
7	DQSA[0..7]	DQSA[0..7]
7	-DQSA[0..7]	-DQSA[0..7]
7	MAAA[0..15]	MAAA[0..15]
8	MAAB[0..15]	MAAB[0..15]
8	DQSB[0..7]	DQSB[0..7]
8	-DQSB[0..7]	-DQSB[0..7]

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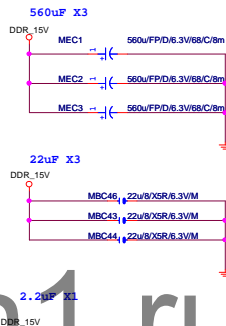
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CPU LGA1150-B			
Size	Document Number	Rev	
Custom	GA-Z97X-UD7 TH	1.0	
Date:	Friday, May 09, 2014	Sheet	5 of 49



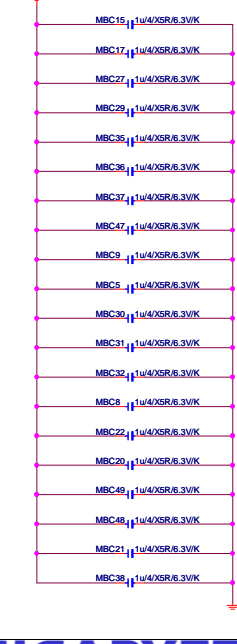
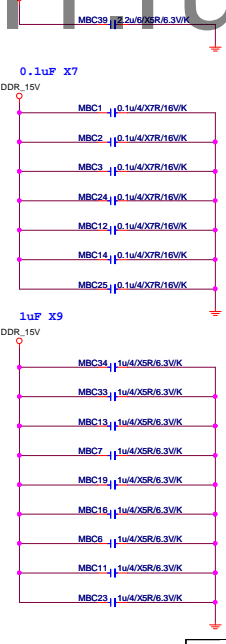
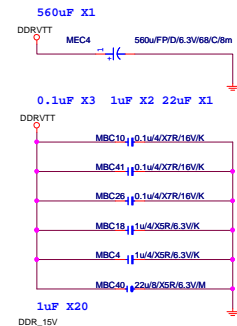


DDR TERMINATION CHANNEL A/B

DDR15V Decouple



DDRVTT Decouple



File

DDR3 CHANNEL A

Size

Document Number

Custom

GA-Z97X-UD7 TH

Date:

Friday, May 08, 2014

Sheet

7

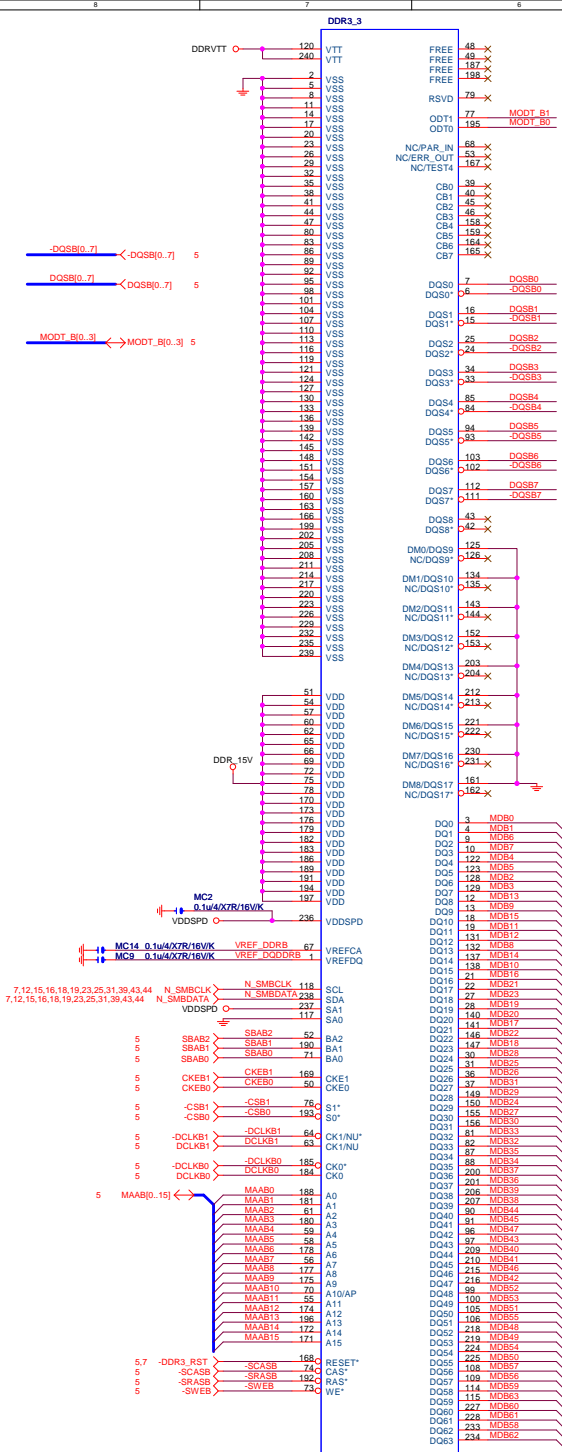
of

48

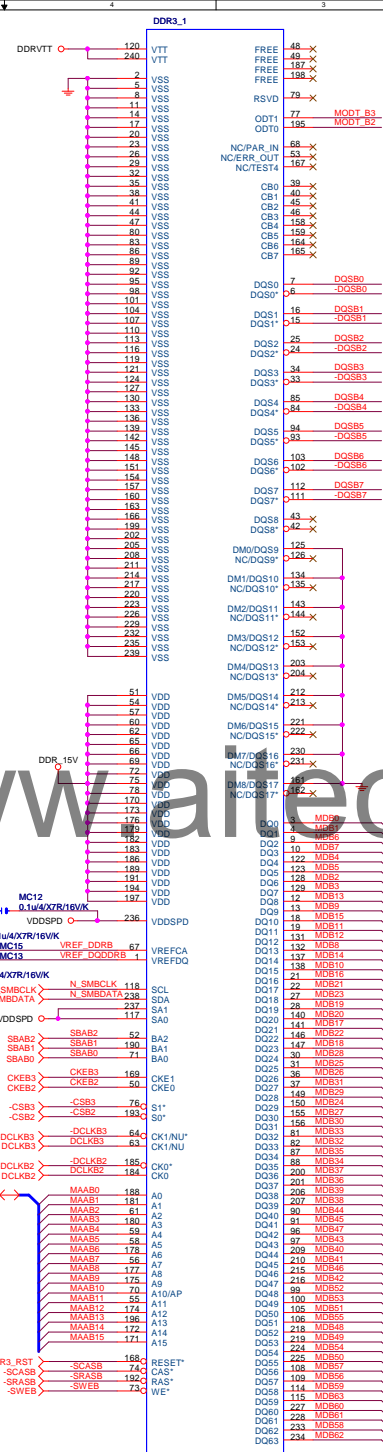
Rev

1.0

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DDR3/240/BK/VA/D



DDR3/240/GR/VA/D



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File: **DDR3 CHANNEL B**

Size: **Document Number**

Custom: **GA-Z97X-UD7 TH**

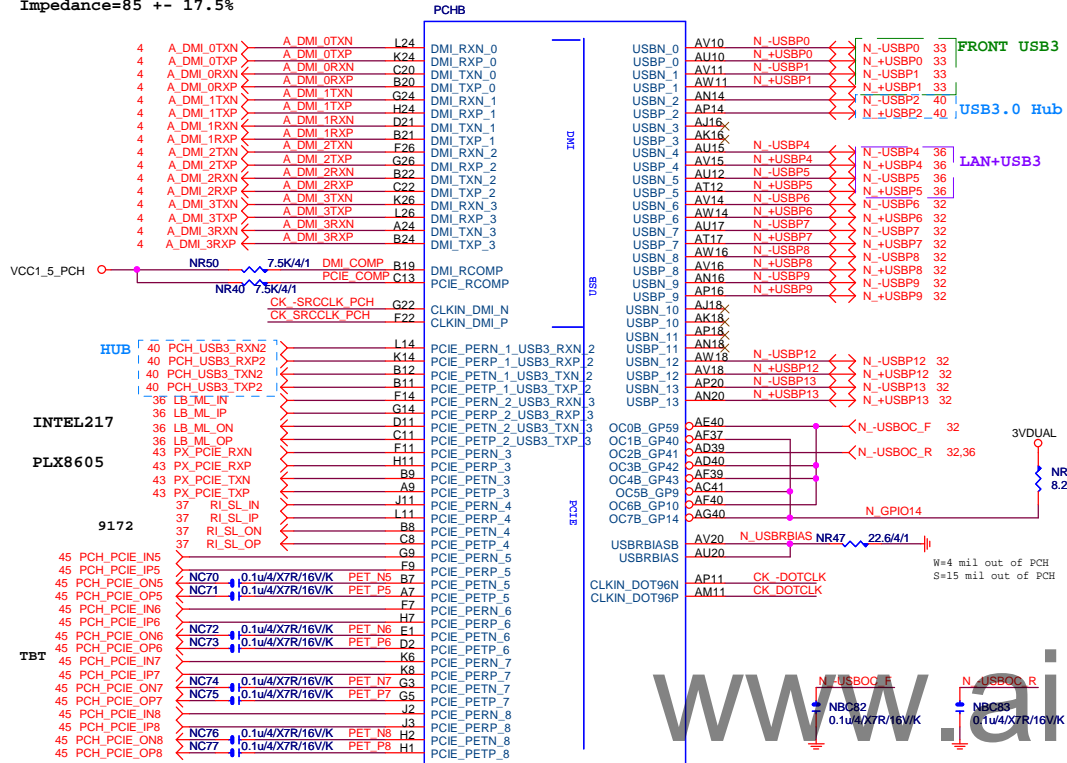
Date: **Friday, May 09, 2014**

Sheet: **8** of **48**

Rev: **1.0**

PCH (B)

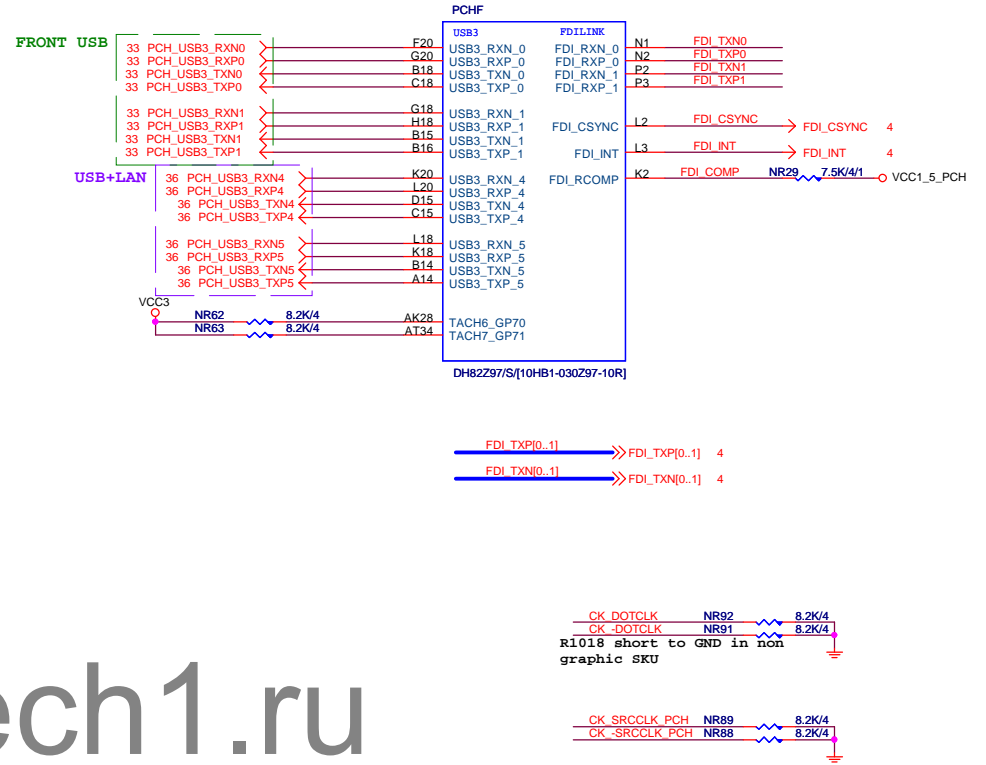
DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%



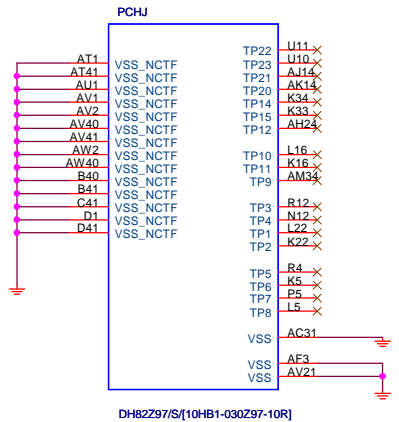
DH82Z97/S/[10HB1-030Z97-10R]

PCH (F)

USB3.0 : 20/5/7/5/20 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

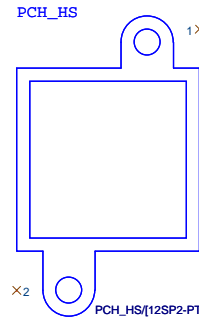


PCH (J)



DH82Z97/S/[10HB1-030Z97-10R]

PCH H/S



PCH_HS/[12SP2-PTZ977-01R_12SP2-PTZ977-02R_12SP2-PTZ977-03R]

USB TABLE

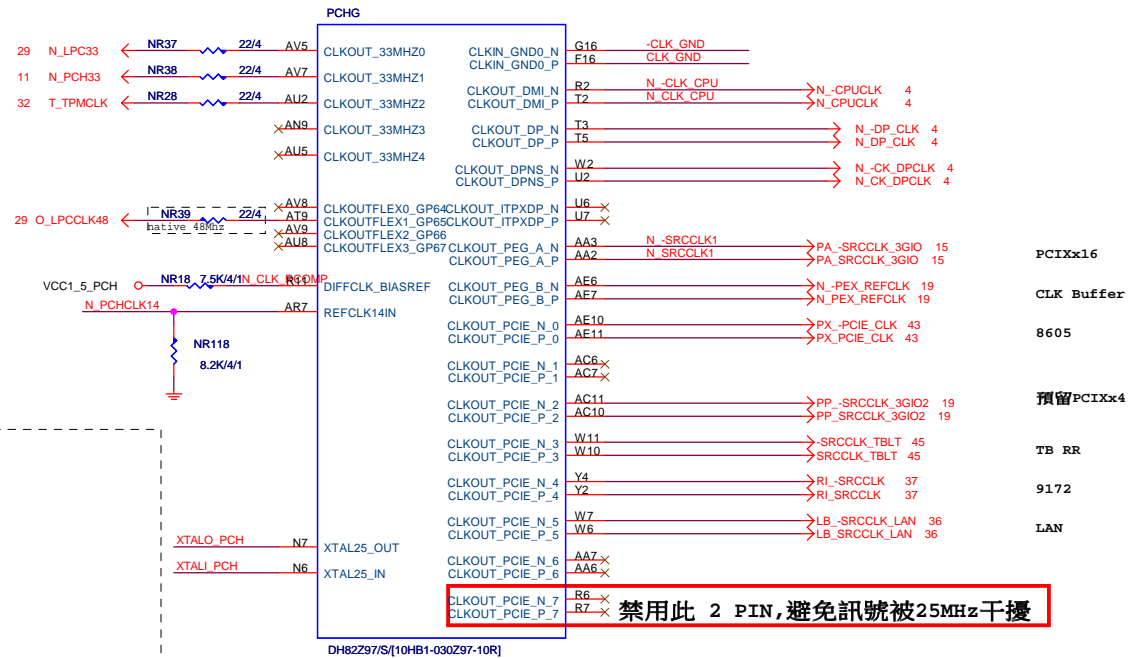
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

	USB PORT	LOCATION	FRONT/Rear
OCB0(0.1)	0.1	F_USB30	FRONT
OCB1(2.3)	2	R_USB30&KB_MS_USB3	Rear(HUB)
OCB2(4.5)	4.5	USB30_LAN	Rear
OCB3(5.6)	6.7	F_USB3	FRONT
OCB4(8.9)	8.9	F_USB2	FRONT
OCB5(10.11)	NA	NA	NA
OCB6(12.13)	12.13	F_USB1	FRONT
OCB7(14.15)	NA	NA	NA

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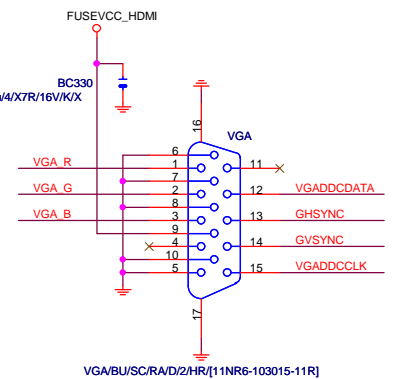
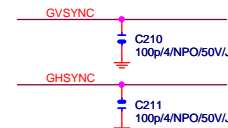
Title	PCH FDI,DMI,USB ,PCIE,NVRAM		
Size	Document Number	Rev	1.0
Custom	GA-Z97X-UD7 TH		
Date:	Friday, May 09, 2014	Sheet	9 of 49

PCH (G)

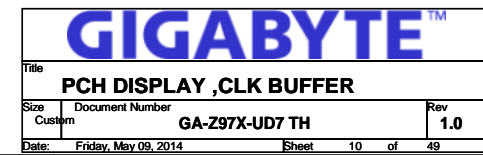
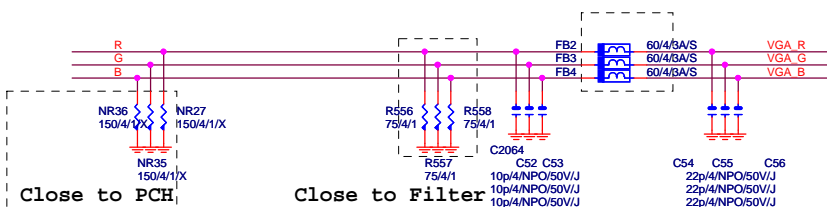


X'TAL 25MHz須參考GND
CRYSTAL/TRACE 週邊不要有訊號,VIA靠近
走線遠離其他40mil以上

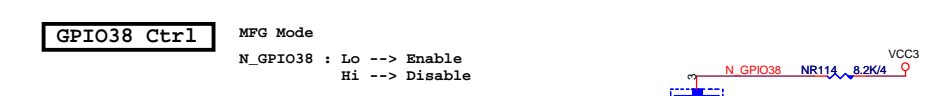
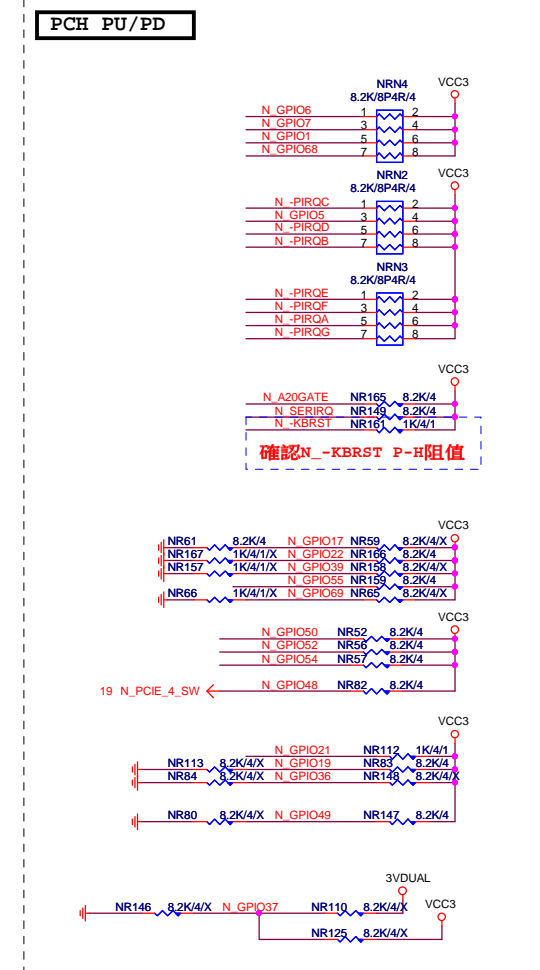
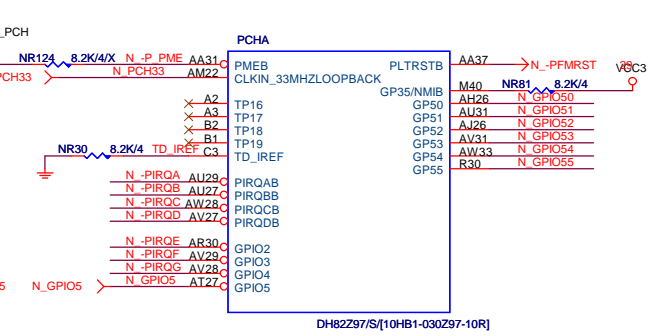
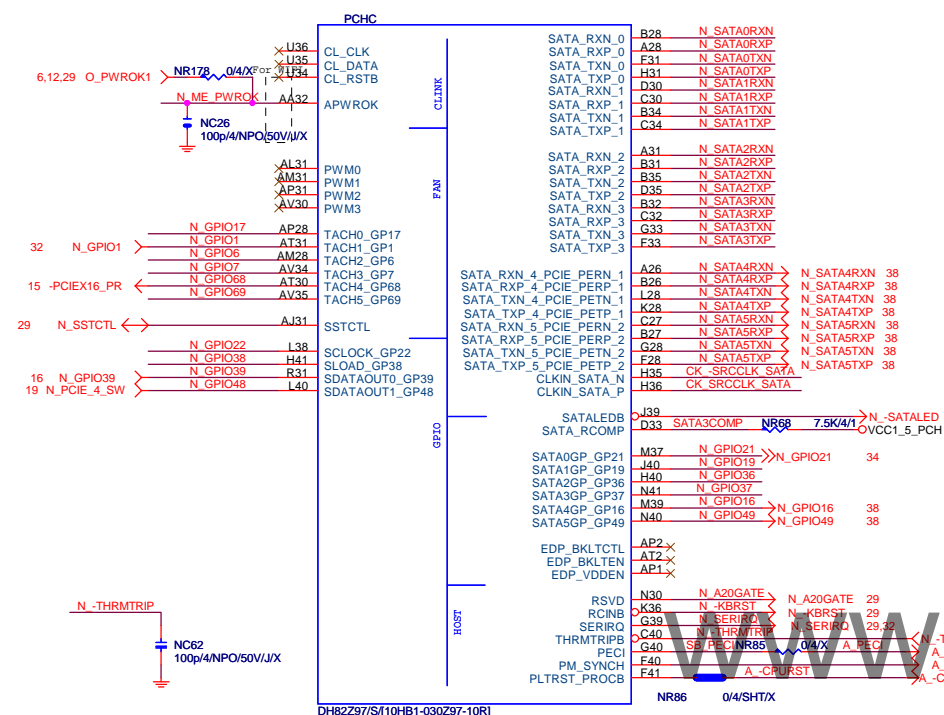
VGA CONNECTOR



VGA DDC



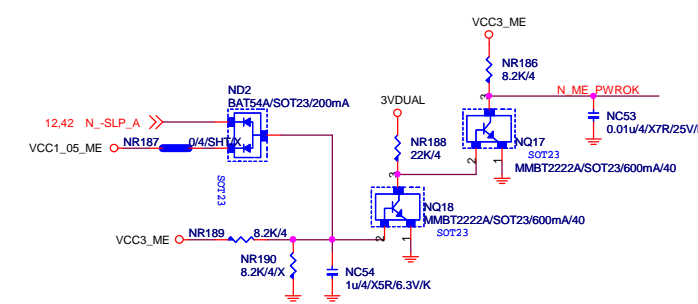
PCH (C)



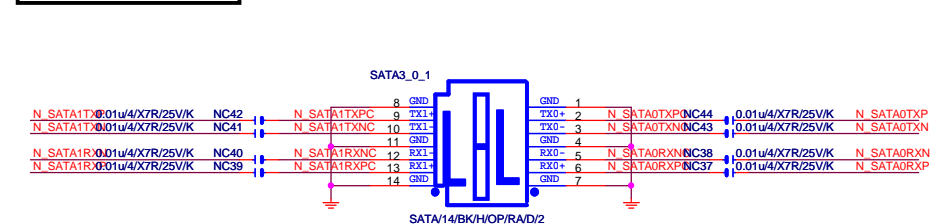
SATA EXPRESS



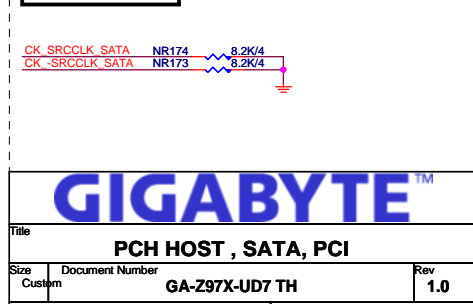
ME PWROK



SATA3 CONNECTOR



PCH CLK PD



GIGABYTE™

Title: PCH HOST, SATA, PCI

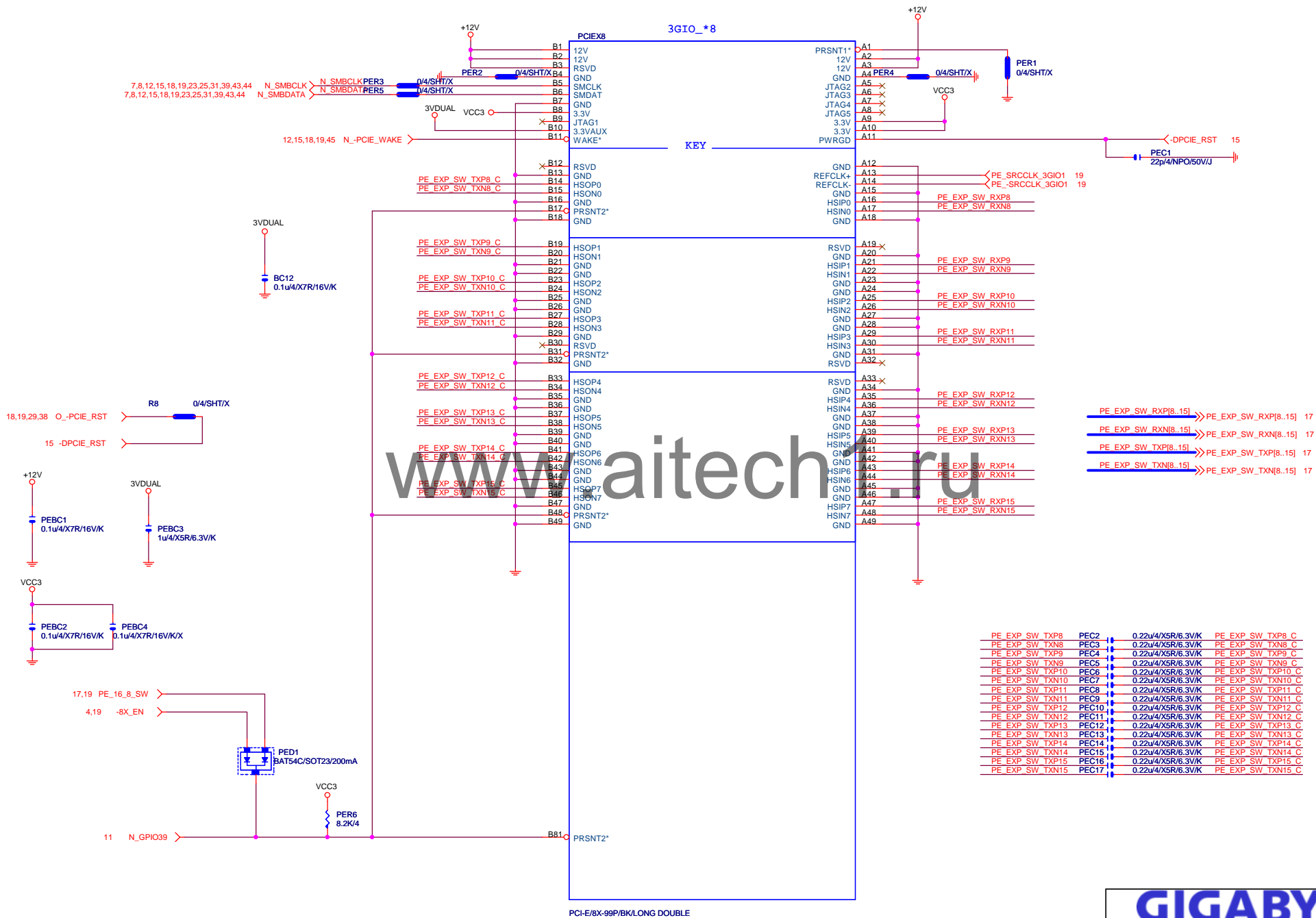
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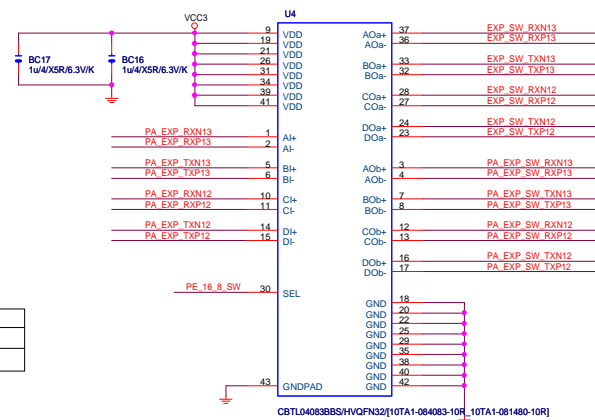
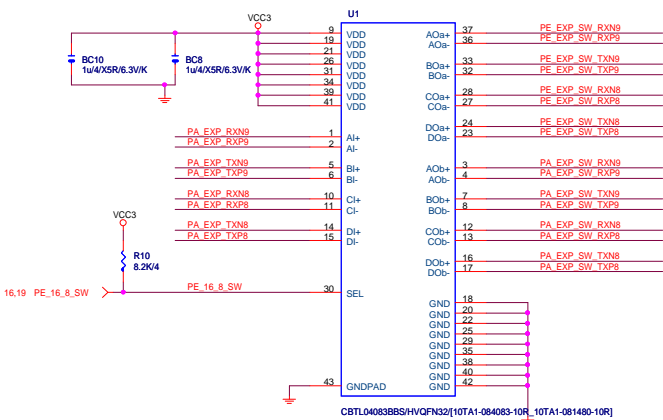
Document Number: GA-Z97X-UD7 TH

Date: Friday, May 09, 2014

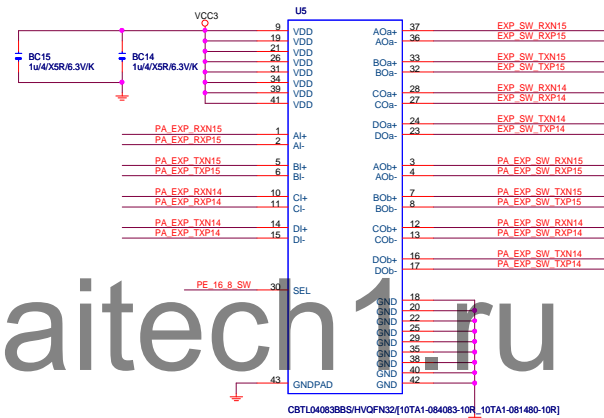
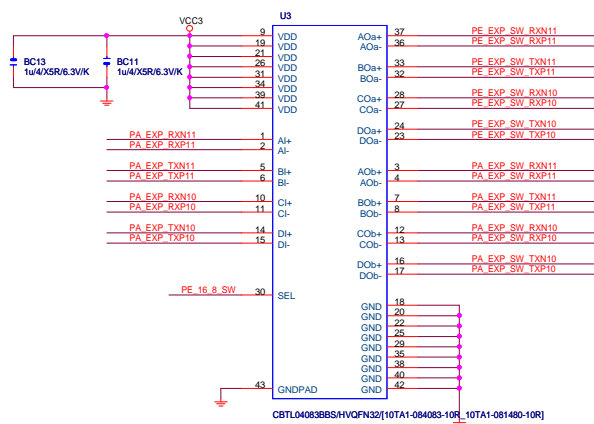
Sheet: 11 of 49

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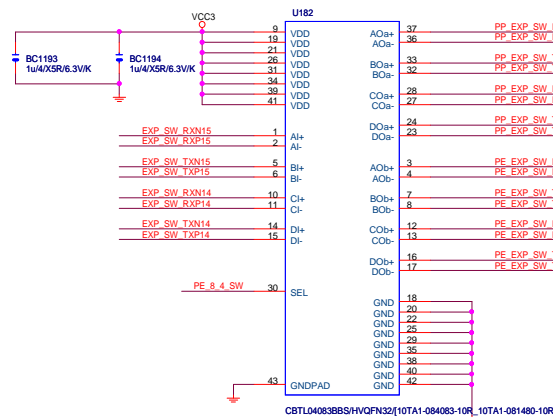
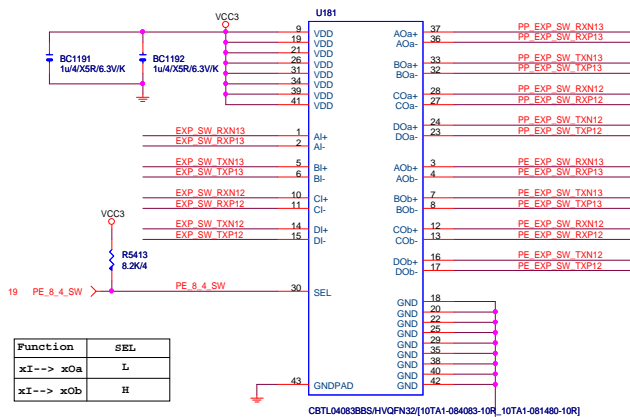




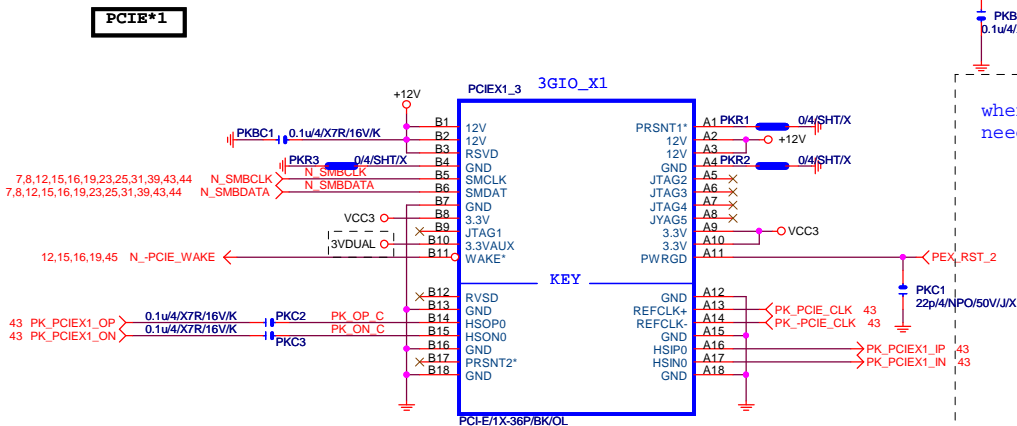
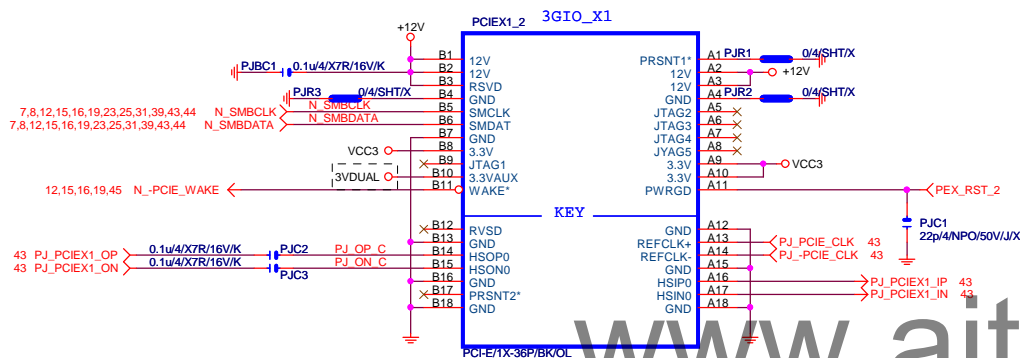
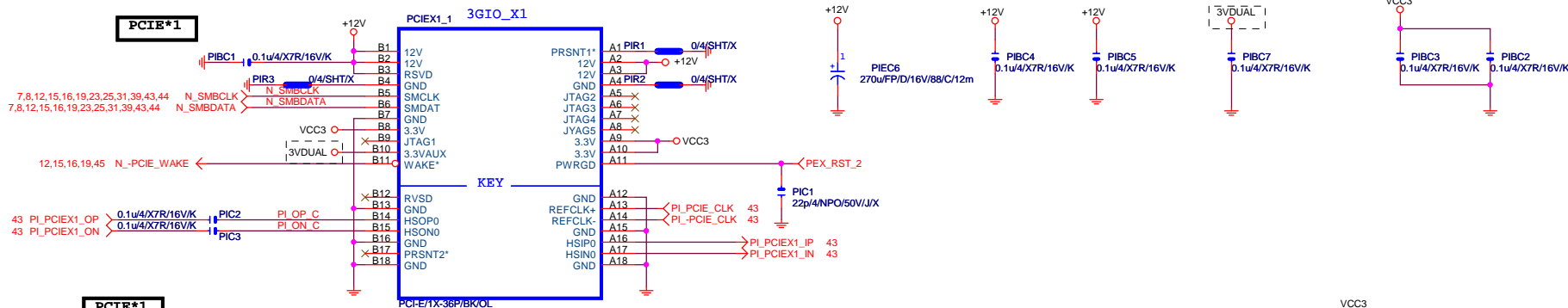
Function	SEL
xI--> x0a	L
xI--> x0b	H



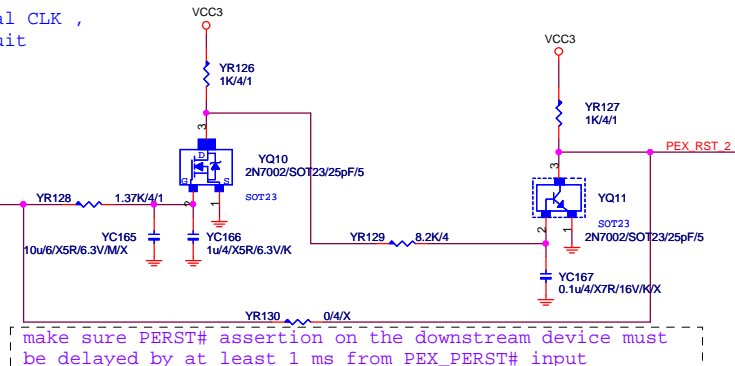
www.aitech.ru



Function	SEL
xI--> x0a	L
xI--> x0b	H



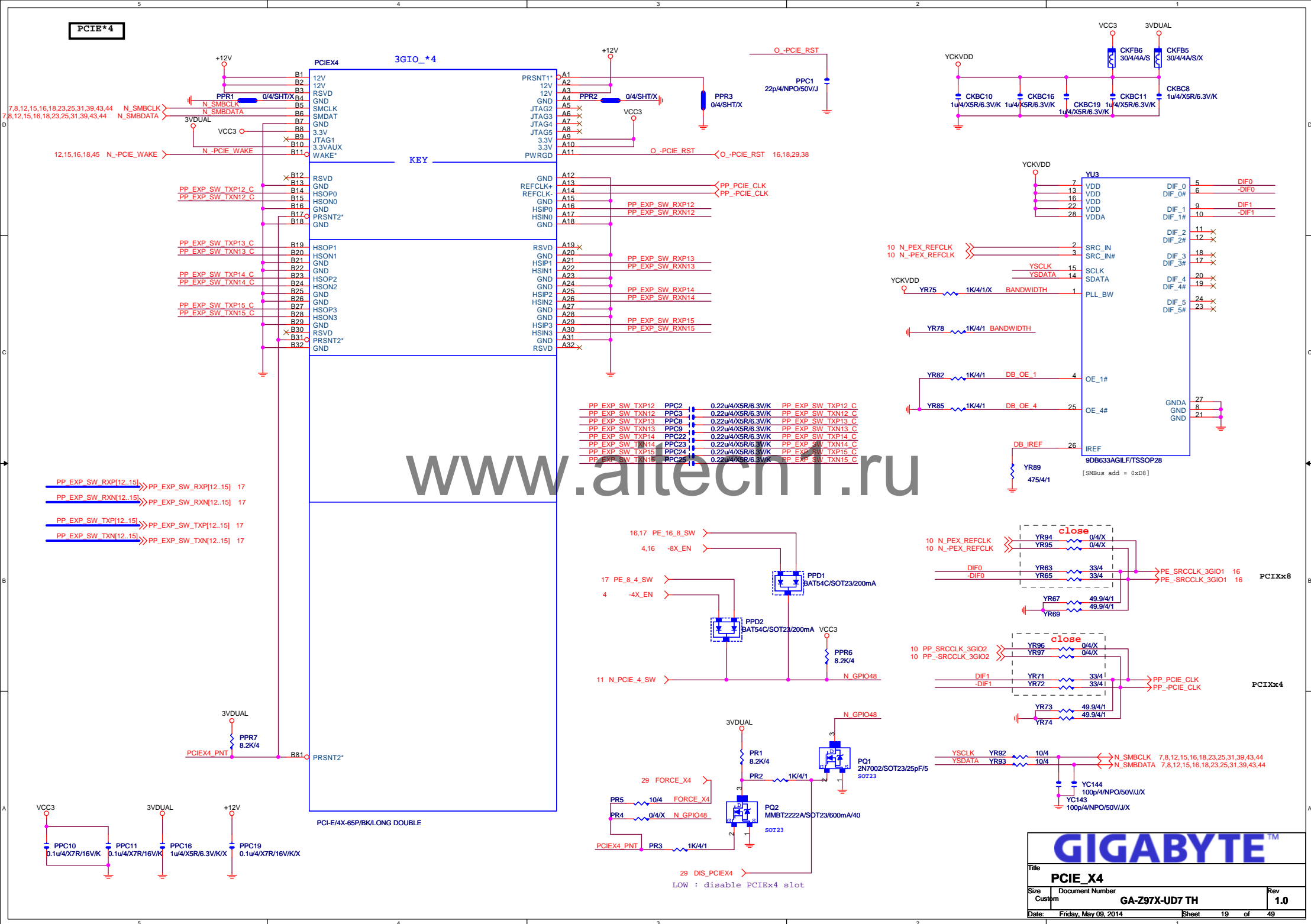
when use 8605 internal CLK ,
need this delay circuit



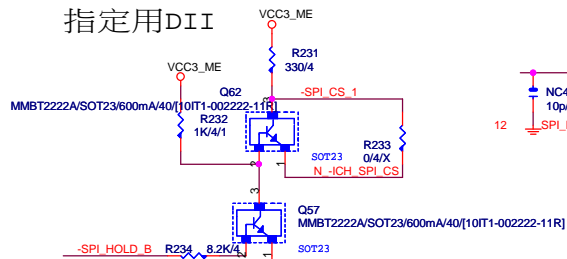
make sure PERST# assertion on the downstream device must
be delayed by at least 1 ms from PEX_PERST# input

GIGABYTE™

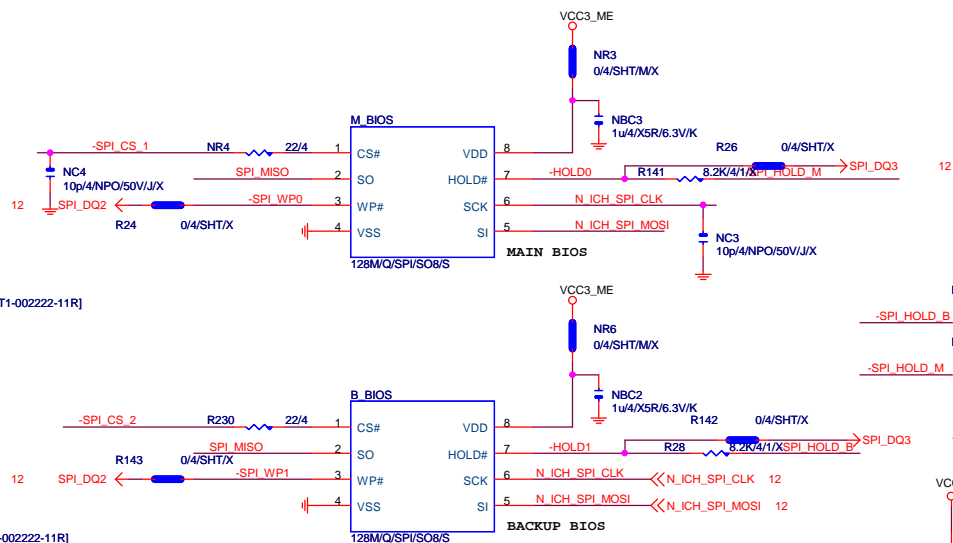
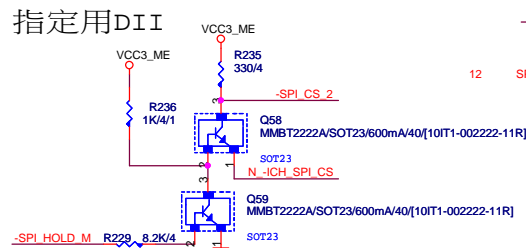
Title			PCIE_X1 1,2,3
Size	Document Number	Rev	
Custom	GA-Z97X-UD7 TH	1.0	
Date:	Friday, May 09, 2014	Sheet	18 of 49



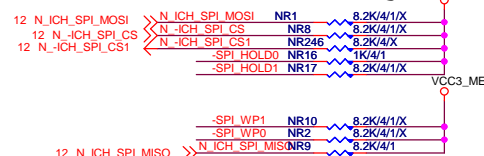
指定用DII



指定用DII



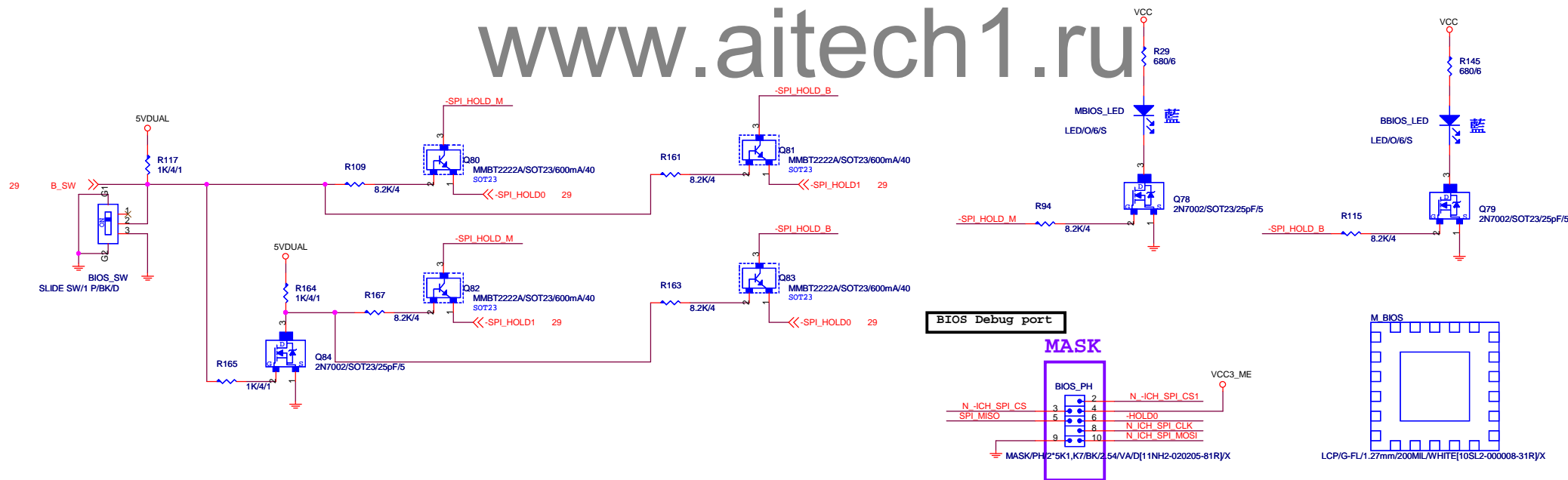
MOSI For DMI RX Termination Voltage



1 means floating
0 means PD 1K

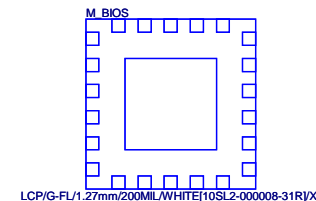
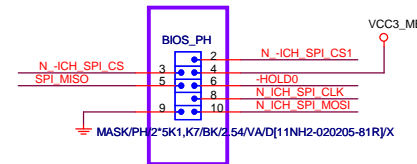
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

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BIOS Debug port

MASK



SB:Single BIOS

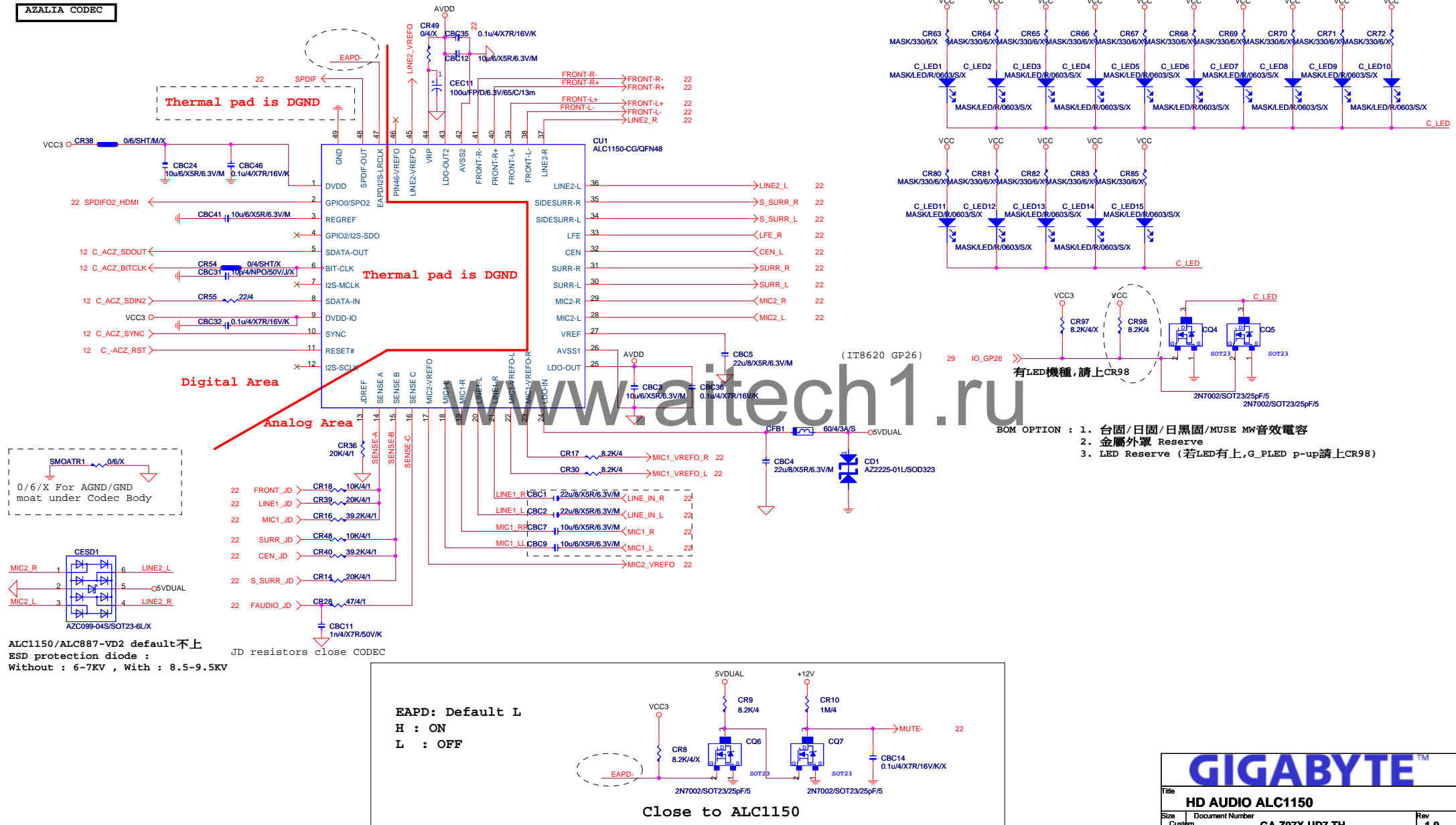
1	Disable
2	Enable

GIGABYTE

DUAL BIOS, TPM

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Size	Custom	1.0
Date:	Friday, May 09, 2014	Sheet 20 of 49

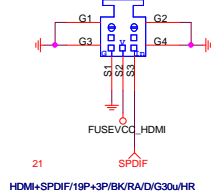
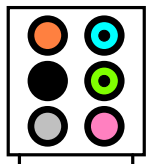
AZALIA CODEC



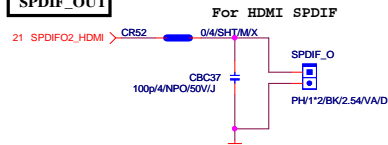
GIGABYTE™

Title			HD AUDIO ALC1150
Size	Document Number	Rev	
Custom	GA-Z97X-UD7 TH	1.0	
Date:	Friday, May 09, 2014	Sheet	21 of 49

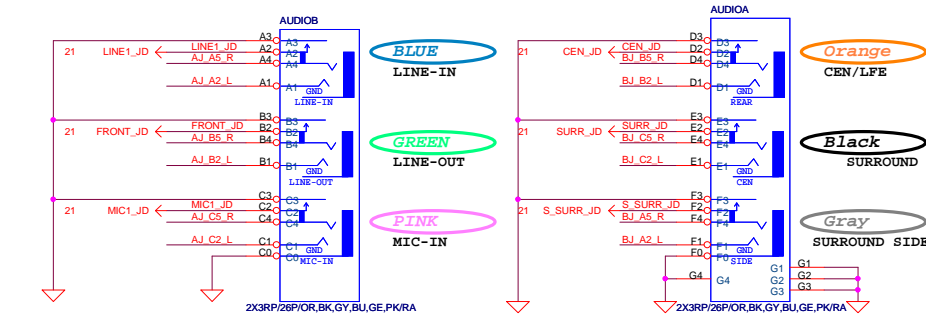
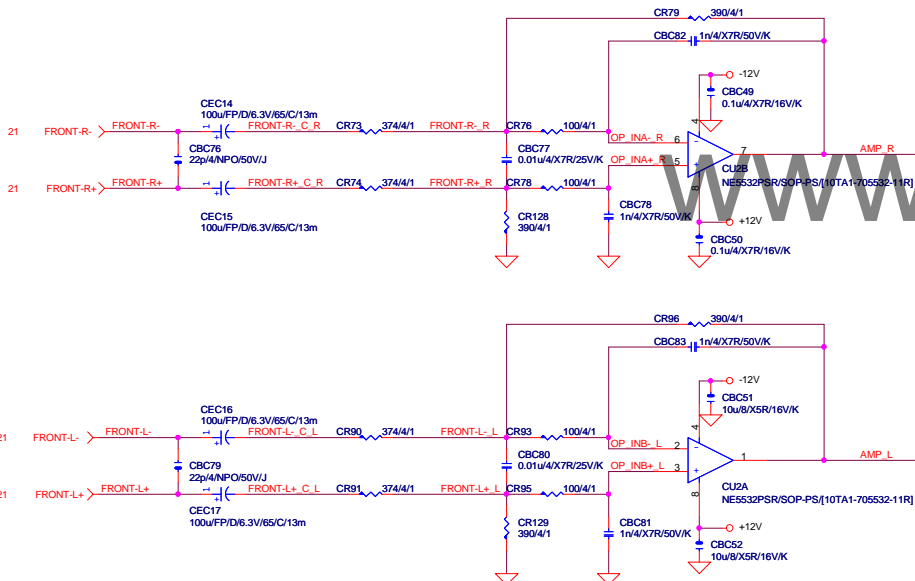
AZALIA JACK



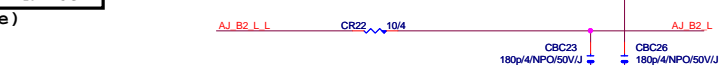
SPDIF_OUT



Differential to Single-End AMPLIFIED



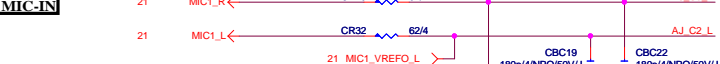
LINE-OUT



LINE-IN



MIC-IN



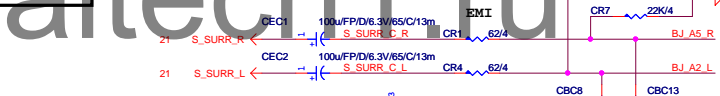
SURROUND



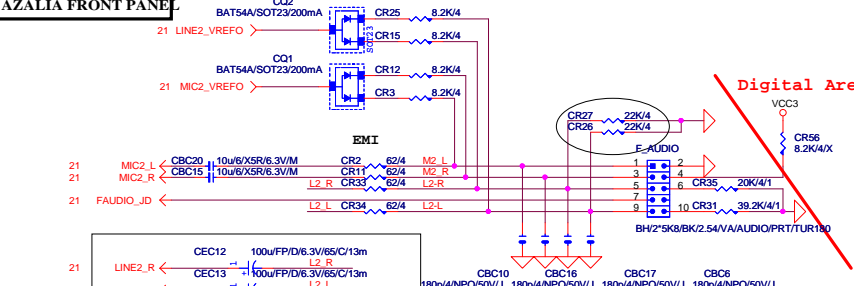
CEN/LFE



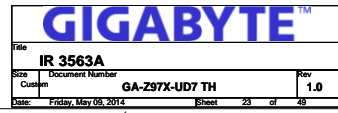
SURR BACK



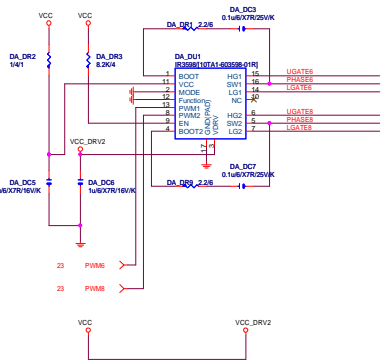
AZALIA FRONT PANEL



Gigabyte Technology			
Title			
AUDIO JACK			
GA-Z97X-UD7 TH			
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Custom			
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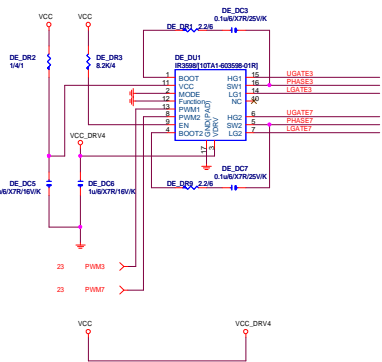
VCORE Phase 6,8



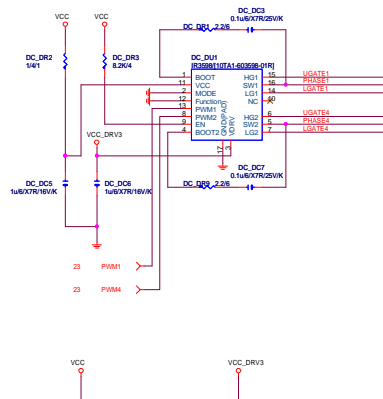
FUNCTION	MODE	PMN MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Sseats	DUAL
1	0	Tri-Sseats	Doubler
OPEN	0	Tri-Sseats	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin1
IC1 pin9 link to IC2 pin9 without PU

VCORE Phase 3,7



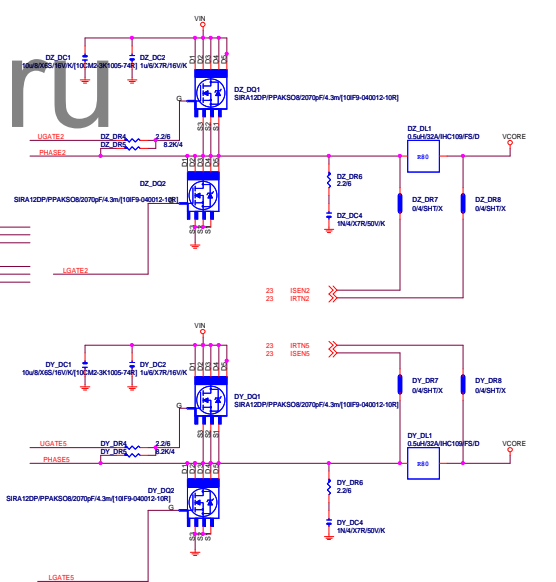
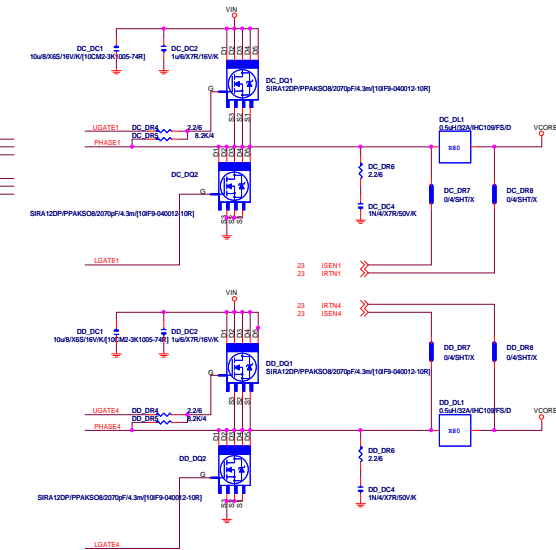
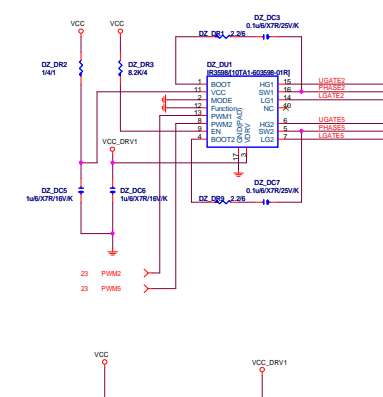
VCORE Phase 1,4

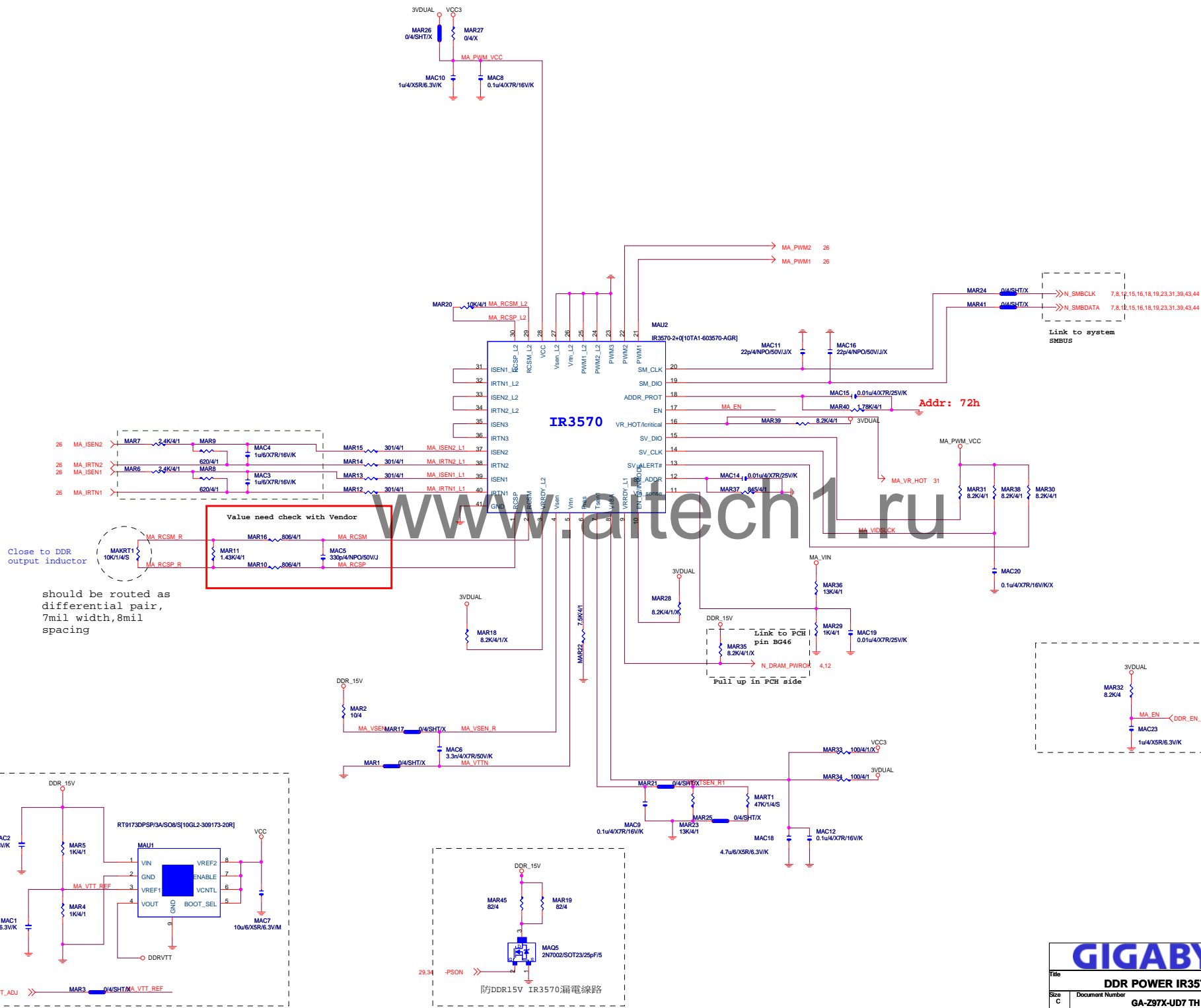


FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IE ATL	DUAL
1	1	IE ATL	Doubler
0	0	Tri-Sate	DUAL
1	0	Tri-Sate	Doubler
OPEN	0	Tri-Sate	Quad
OPEN	1	IE ATL	Quad

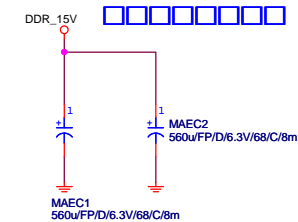
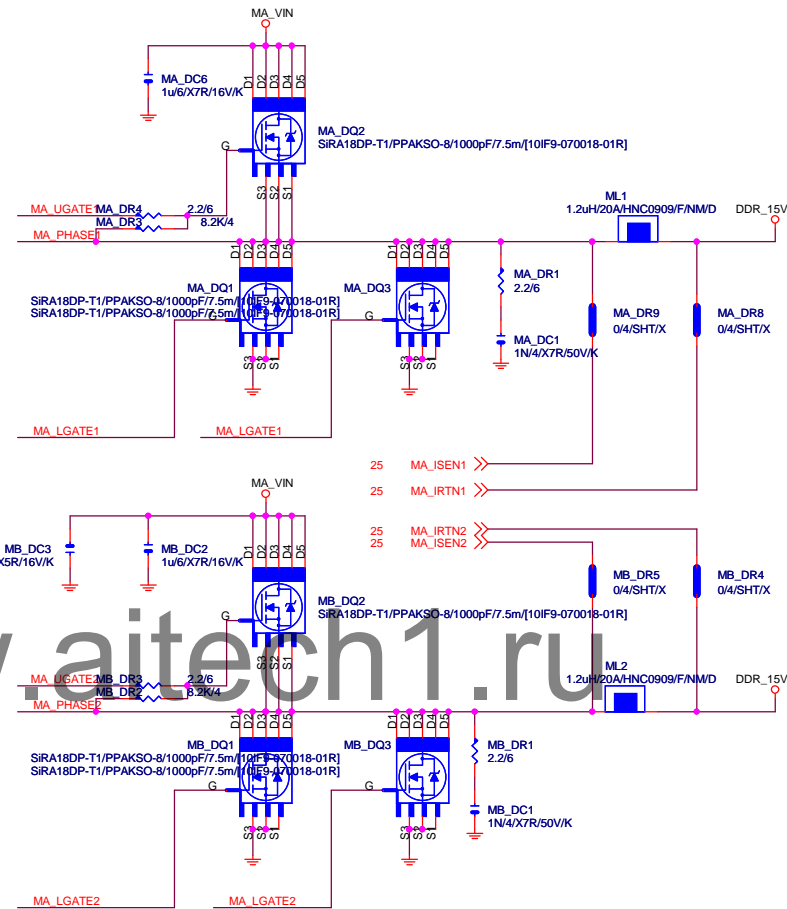
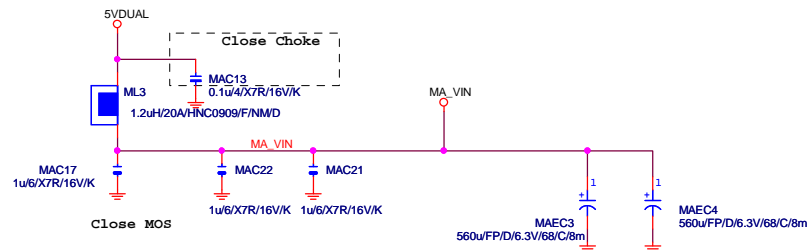
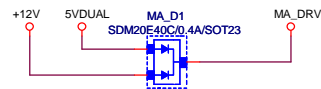
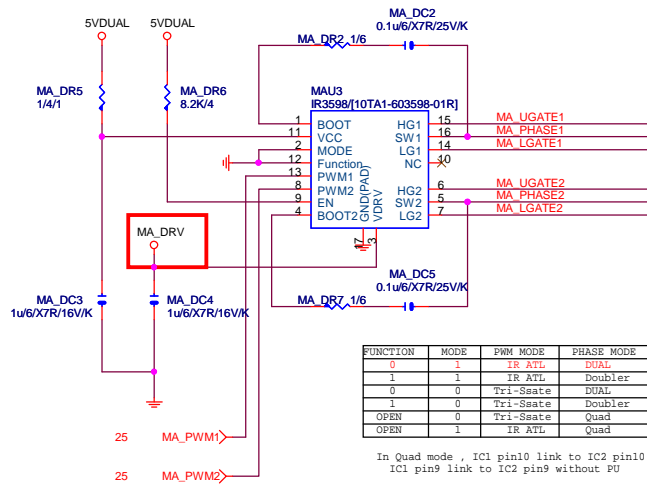
In Quad mode , IC1 pin10 link to IC2 pin1
IC1 pin9 link to IC2 pin9 without SW

VCORE Phase 2,5

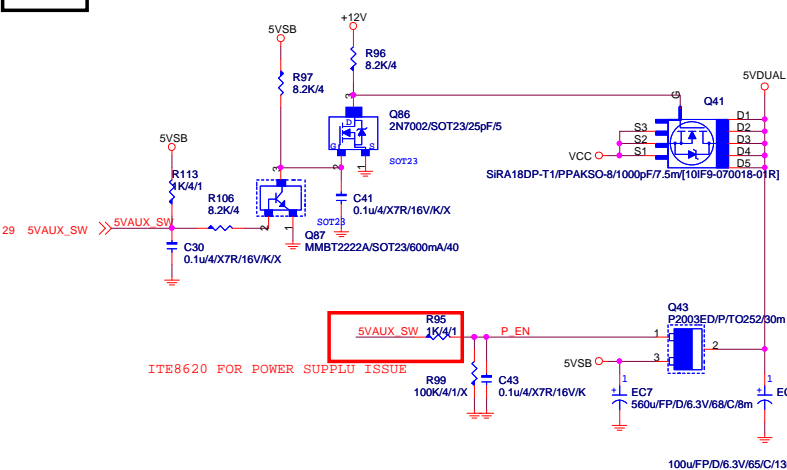




DDR_15V



5VDUAL

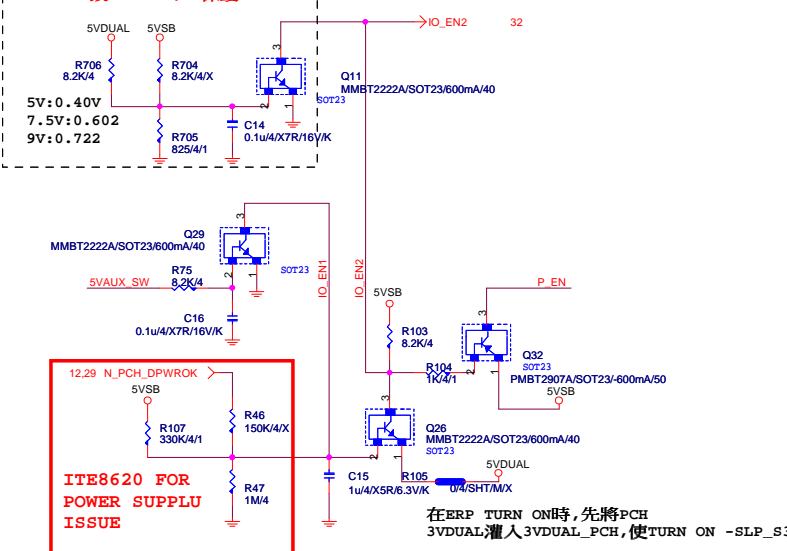


5VDUAL SHORT PROTECT



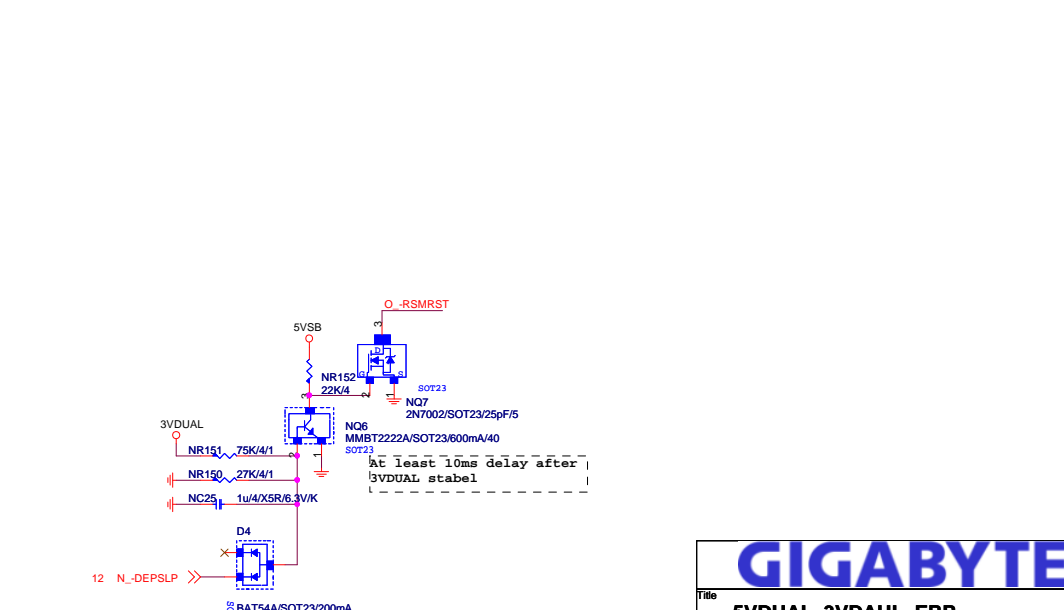
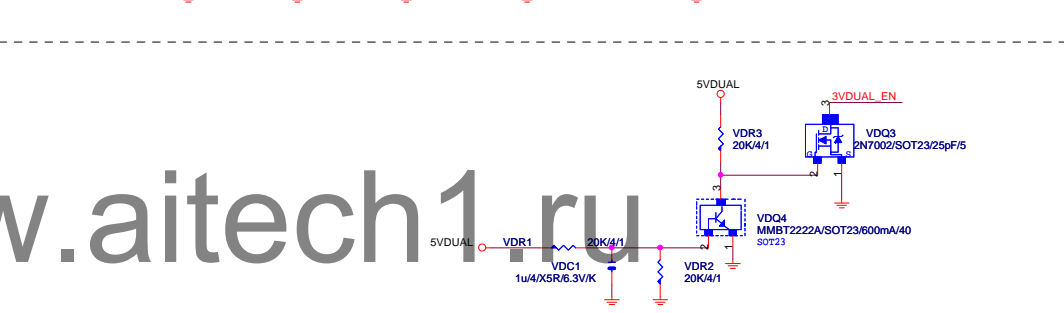
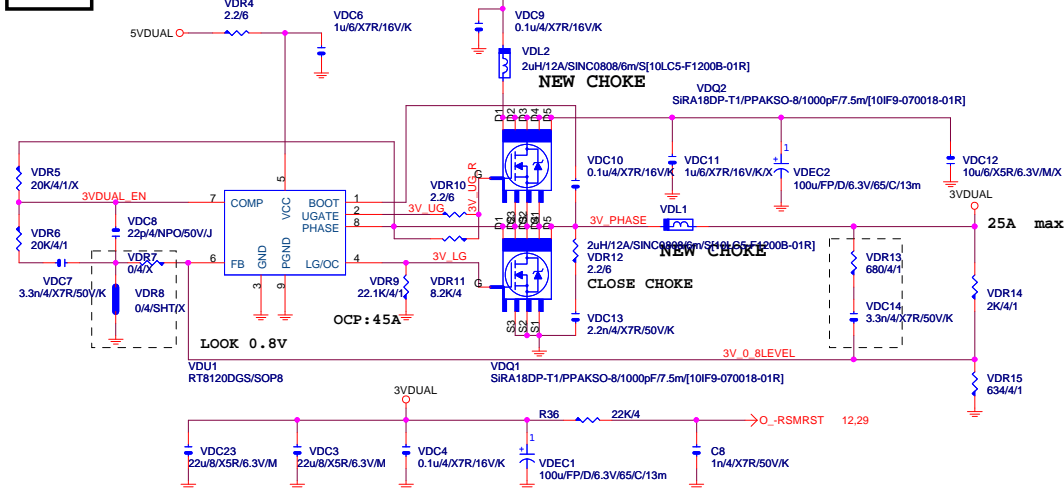
5VSB OVP:7.5V protection

NOTE 82:改5V DUAL,6v保護

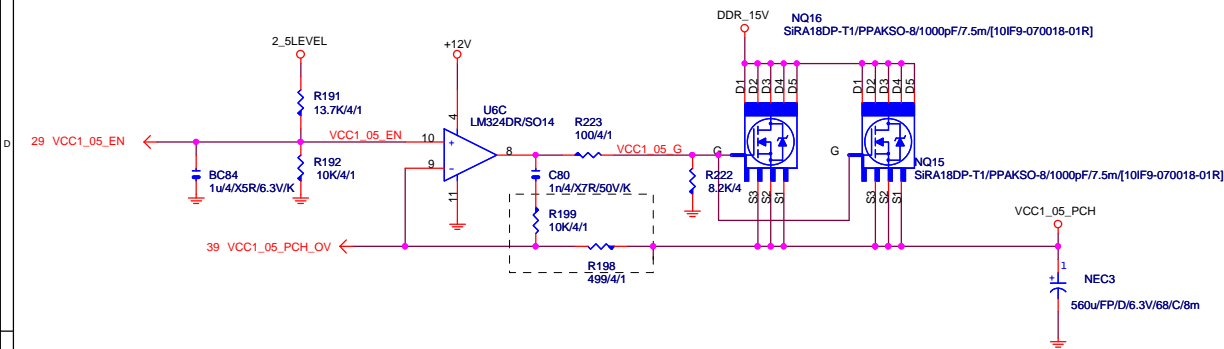


在ERP TURN ON時,先將PCH 3VDUAL灌入3VDUAL_PCH,使TURN ON -SLP_S3功能

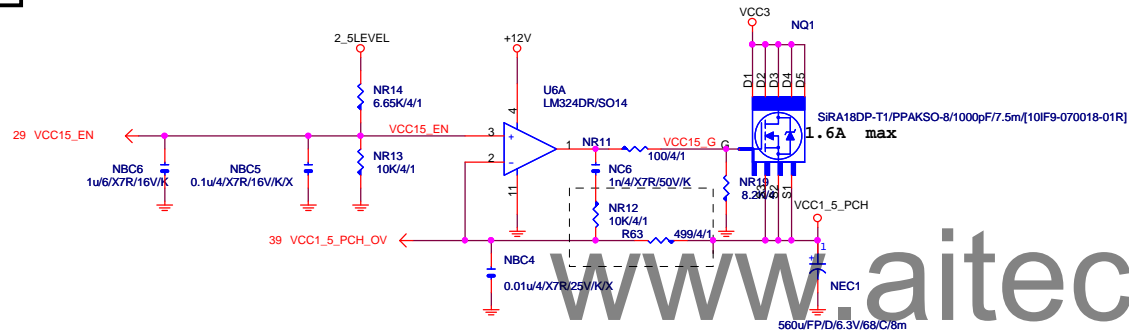
3VDUAL



VCC1_05_PCH



VCC1_5_PCH



Rise/Fall max 50us

Rise:20% - 80%

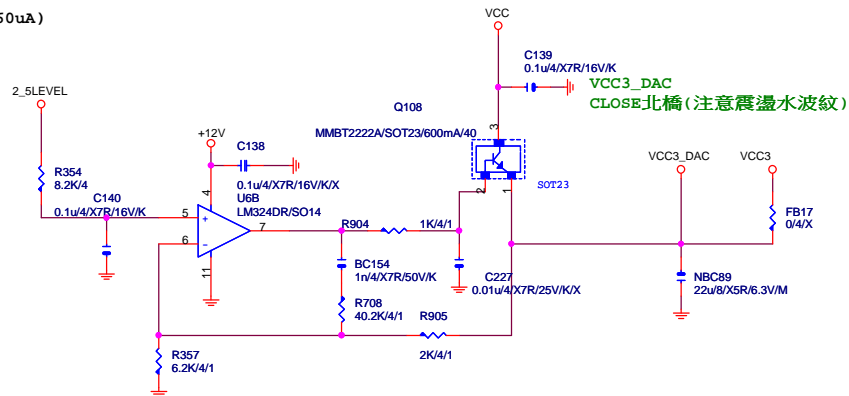
Fall :2V- 0.8V

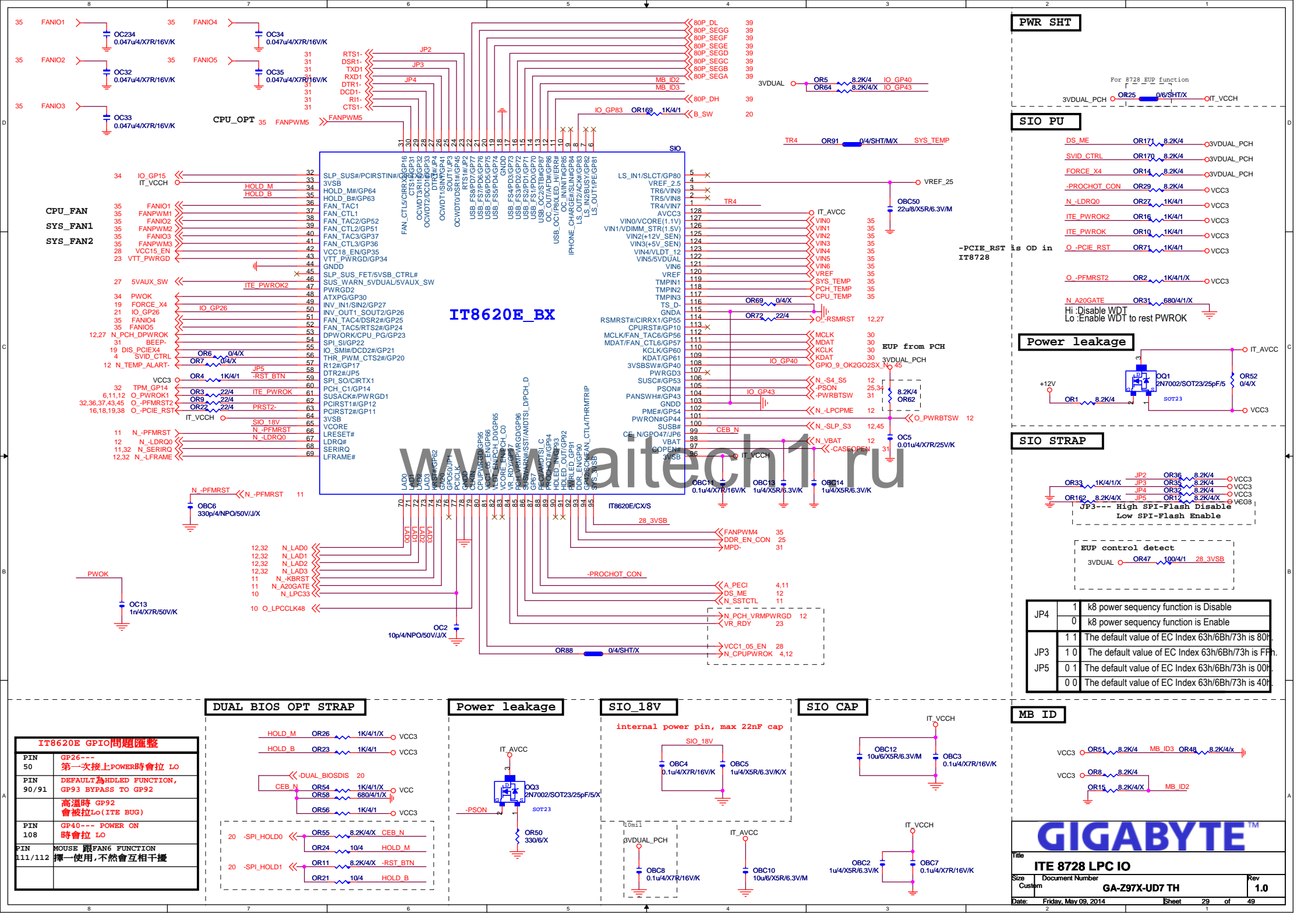
At least 10ms delay after 3VDUAL ready

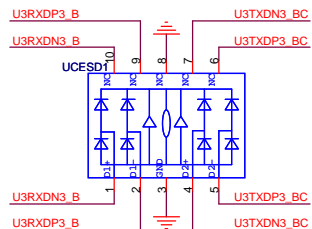
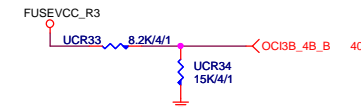
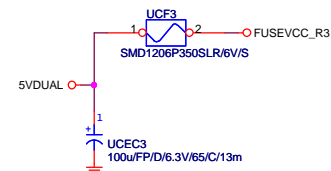
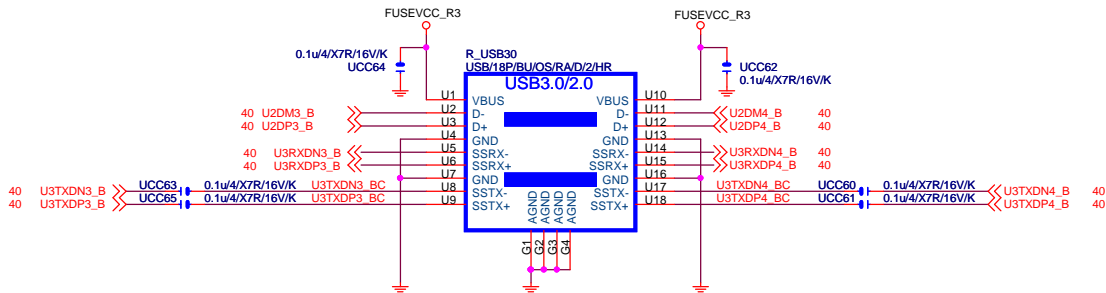
Pop when PCH & SIO both use 3VDUAL-PCH

VCC3_DAC

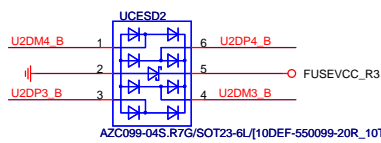
(3.3V/70mA+360uA)



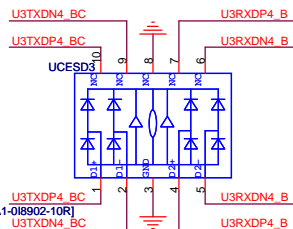




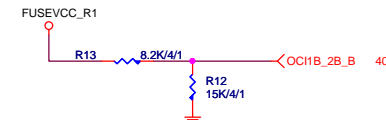
AZ1045-04F/MSOP10
Close to connector



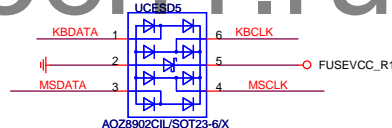
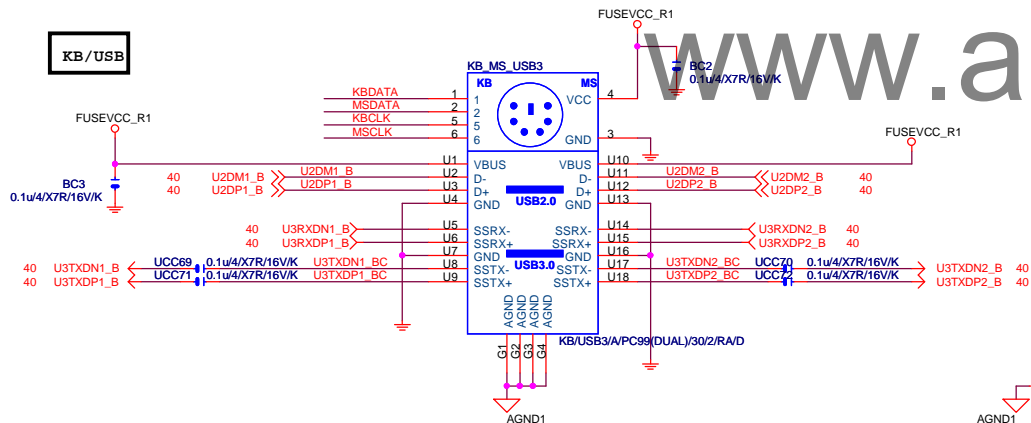
Close to connector



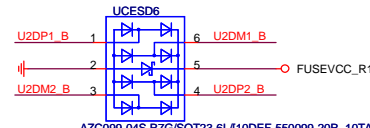
AZ1045-04F/MSOP10
Close to connector



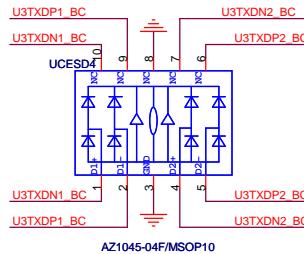
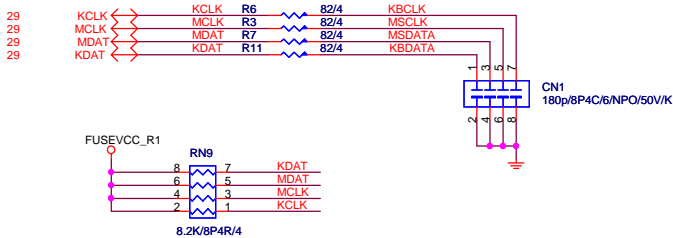
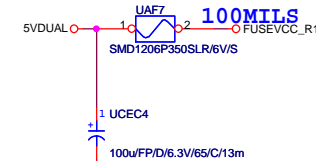
KB/USB



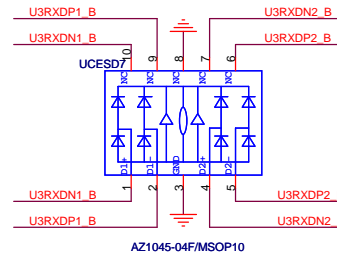
Close to connector



Close to connector



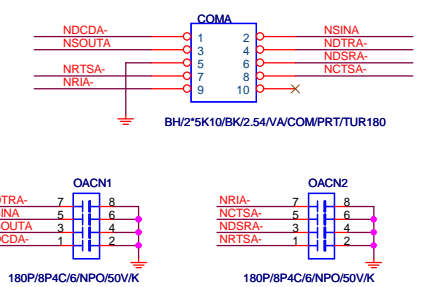
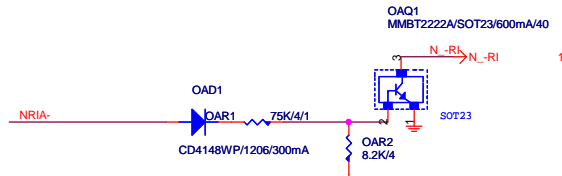
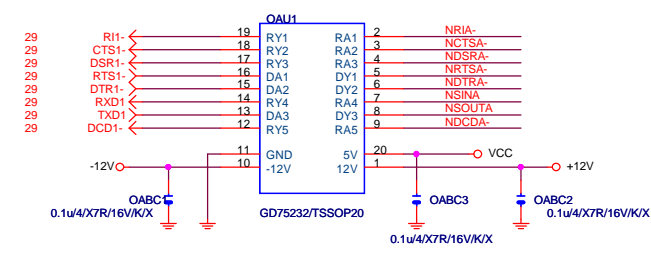
Close to connector



Close to connector

COMA

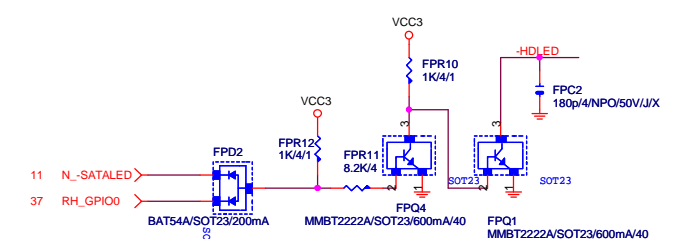
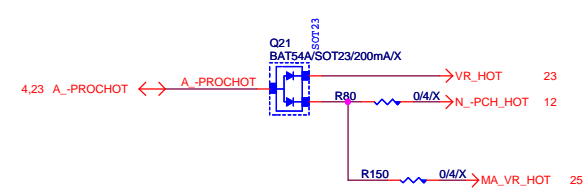
COM RI



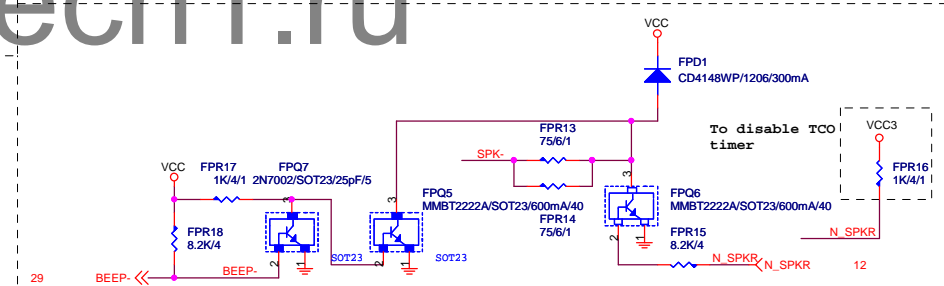
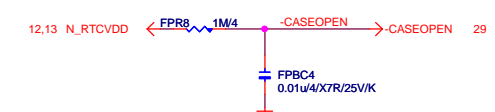
-PROHOT

Thunderbolt

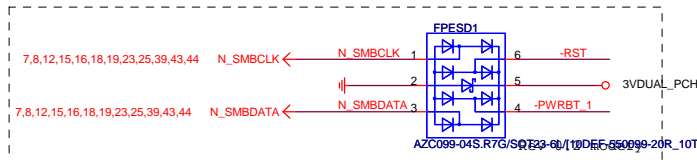
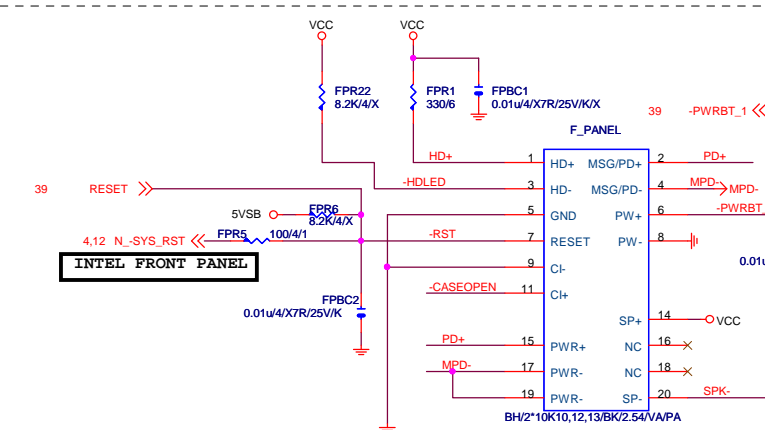
SATA LED



CASE OPEN



INTEL FRONT PANEL



GIGABYTE

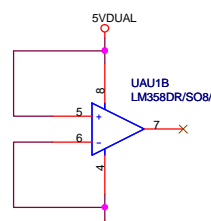
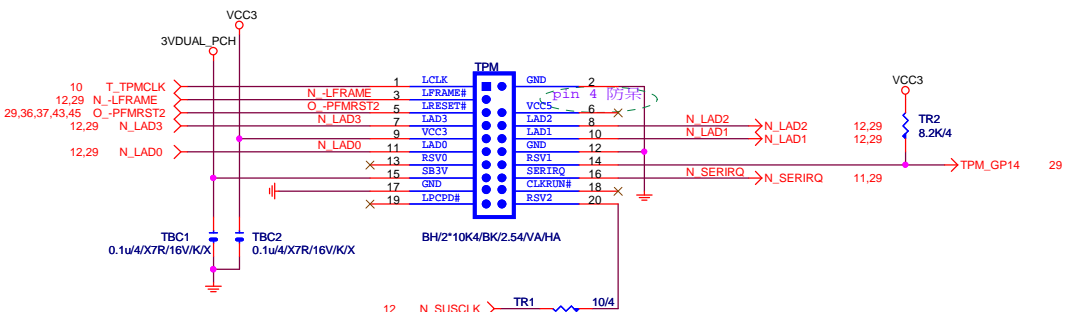
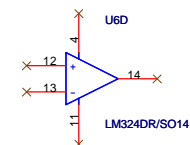
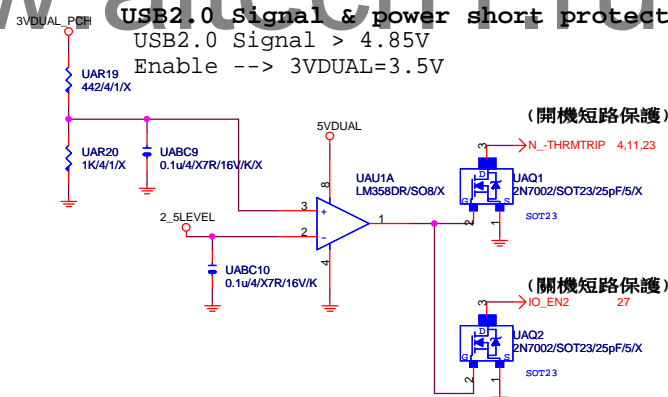
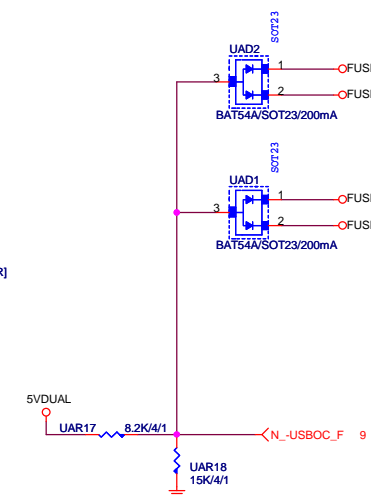
FP, COM, -PHOT

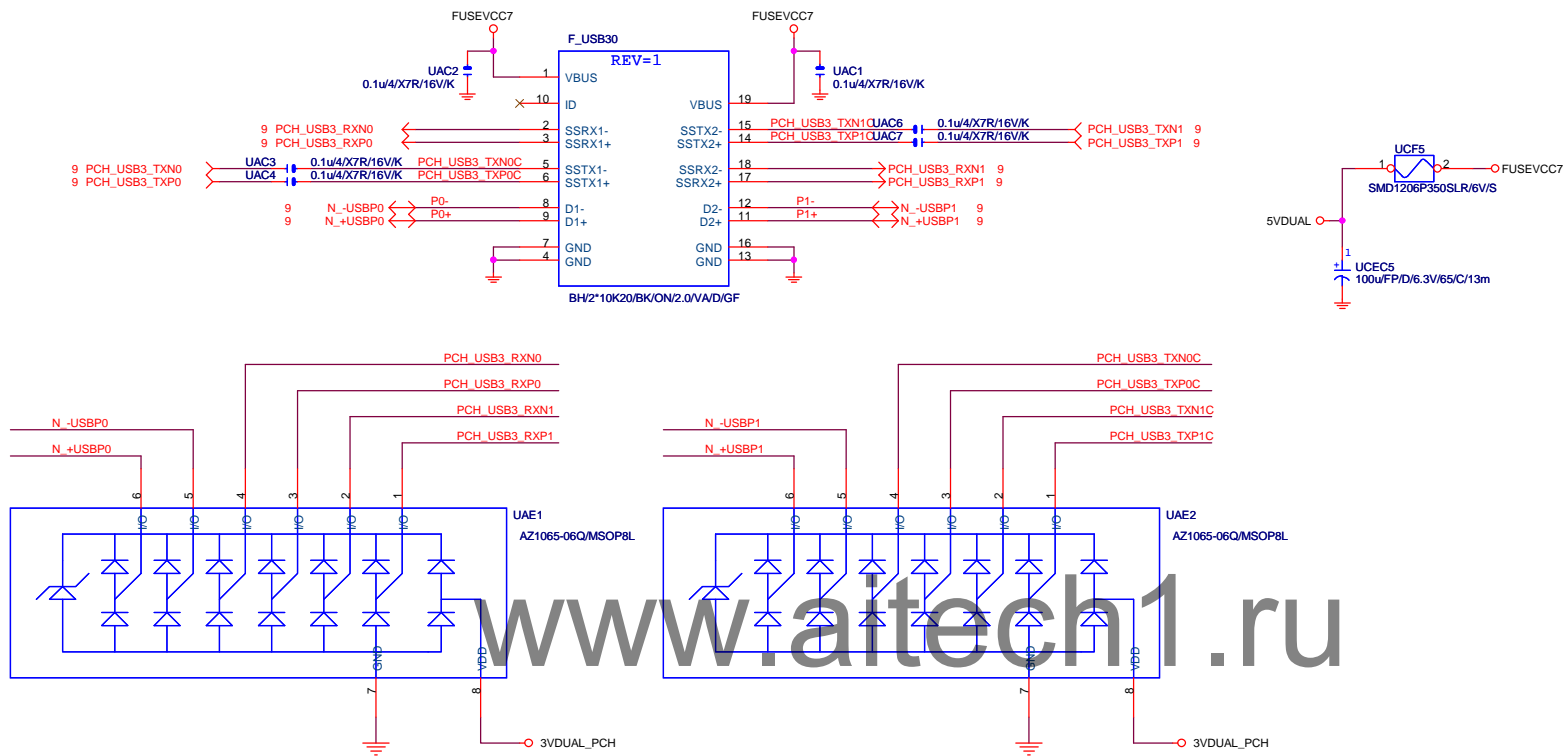
Document Number: **GA-Z97X-UD7 TH**

Rev: **1.0**

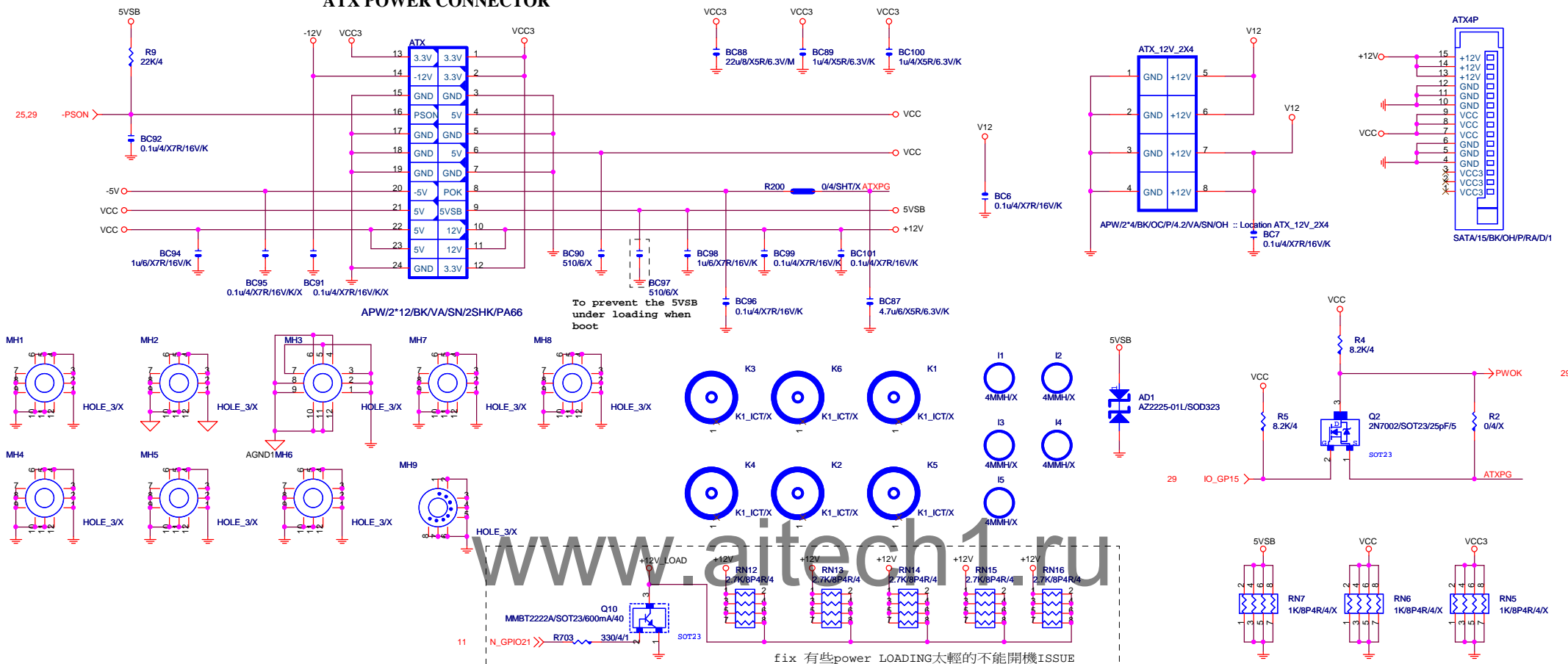
Date: Friday, May 09, 2014

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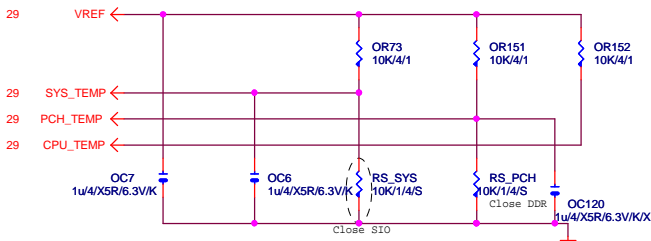




ATX POWER CONNECTOR

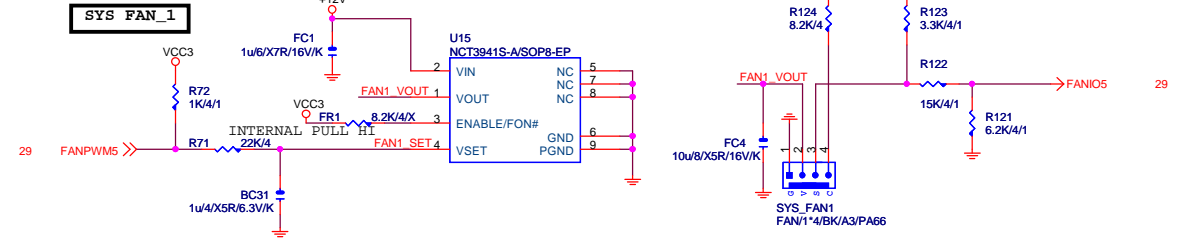


TEMP H/W MONITOR

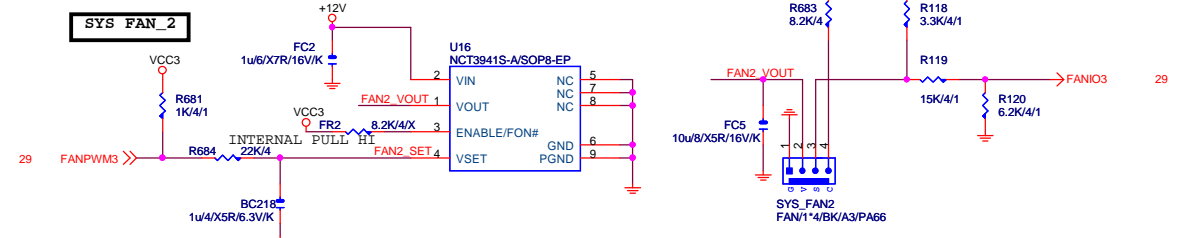


Linear SYS_FAN

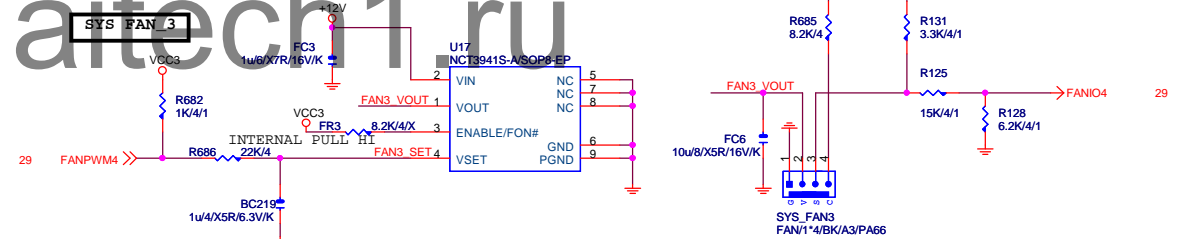
Enable Function (NCT3941S)
Pull Turn On Function (NCT3941S-A)



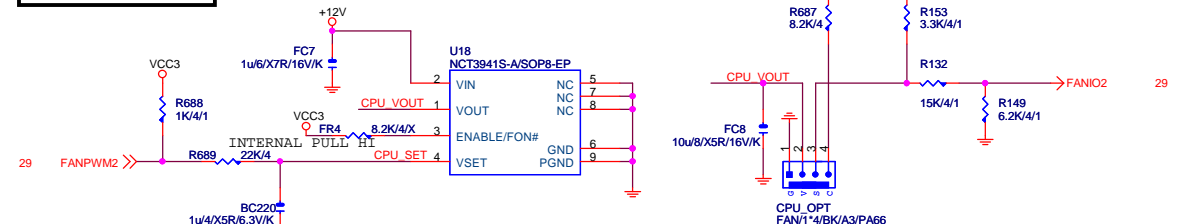
Linear SYS_FAN



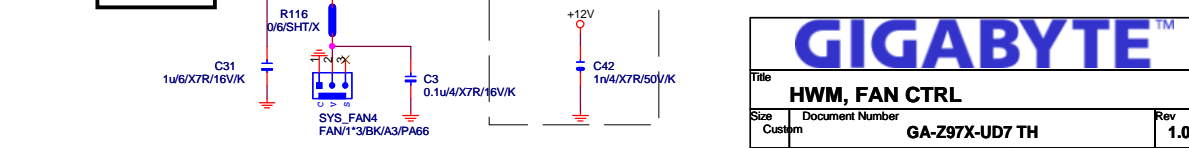
Linear SYS_FAN



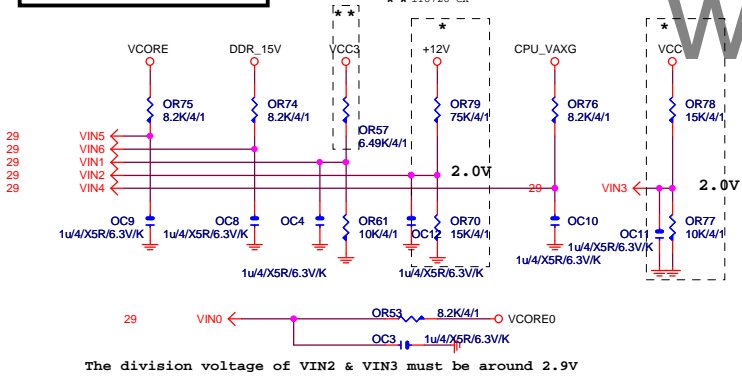
CPU OPT SMART FAN Linear CPU_OPT



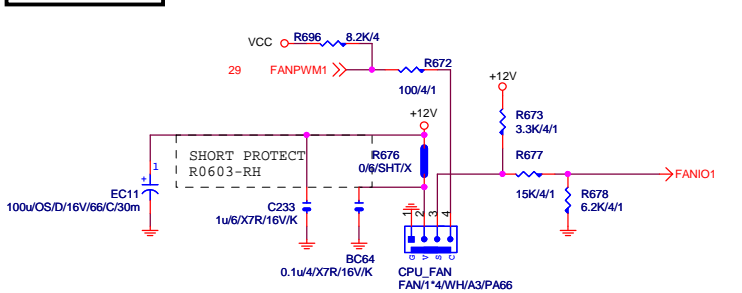
SYS_FAN_4



VOLTAGE-- H/W MONITOR

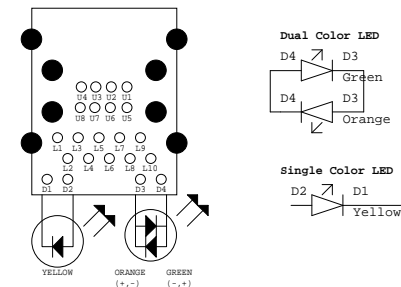
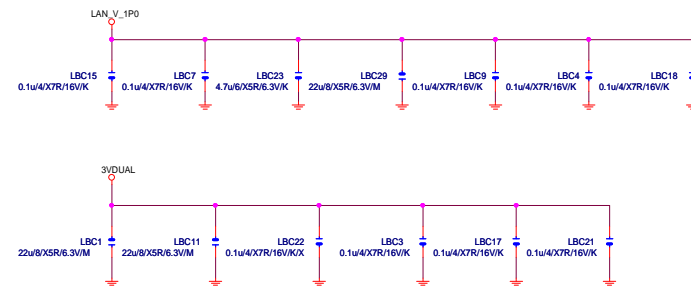


CPU SMART FAN



GIGABYTE™

Title			HWM, FAN CTRL
Size	Document Number	Rev	
Custom	GA-Z97X-UD7 TH	1.0	
Date:	Friday, May 09, 2014	Sheet	35 of 49



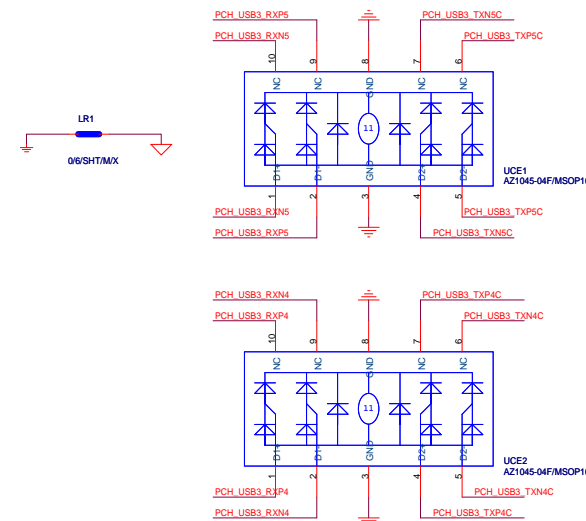
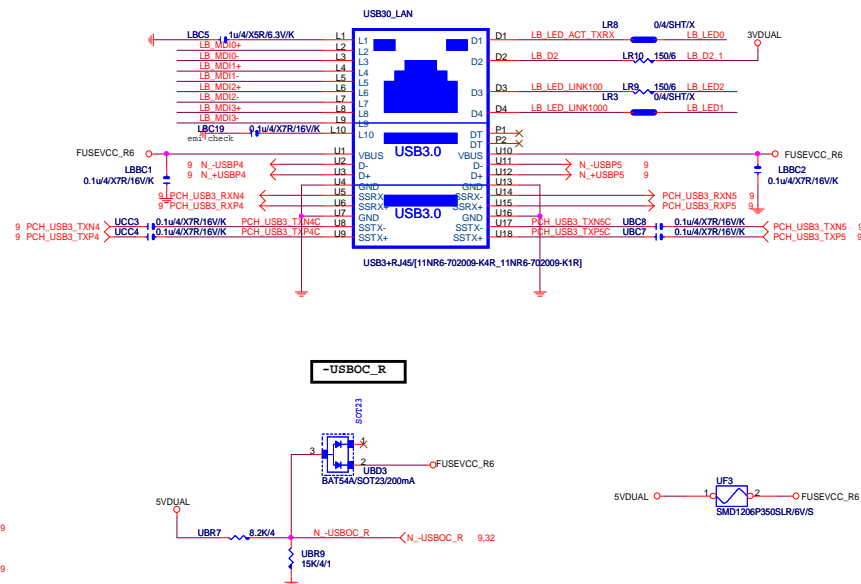
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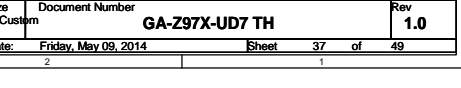
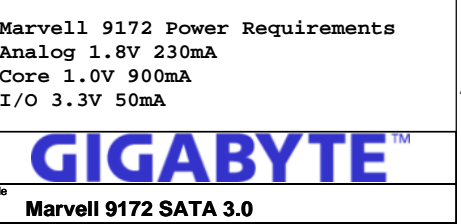
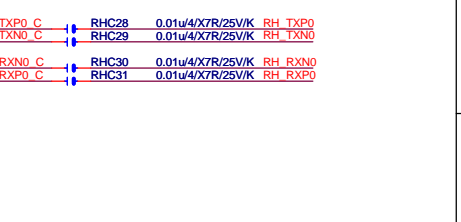
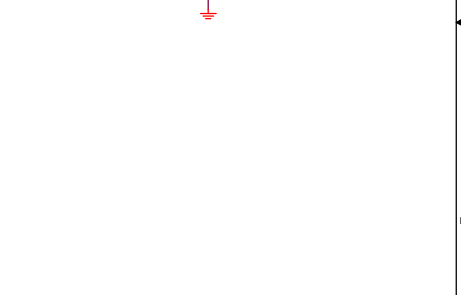
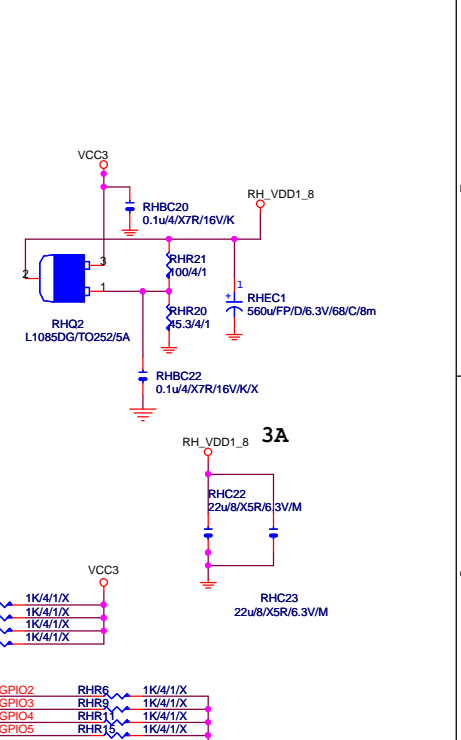
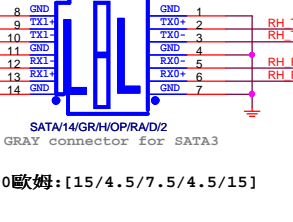
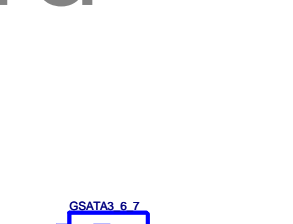
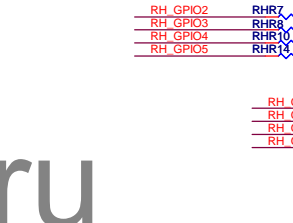
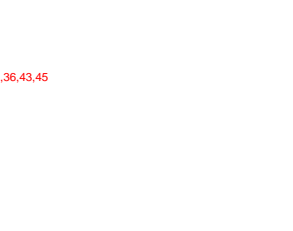
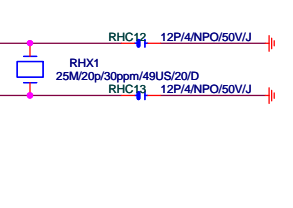
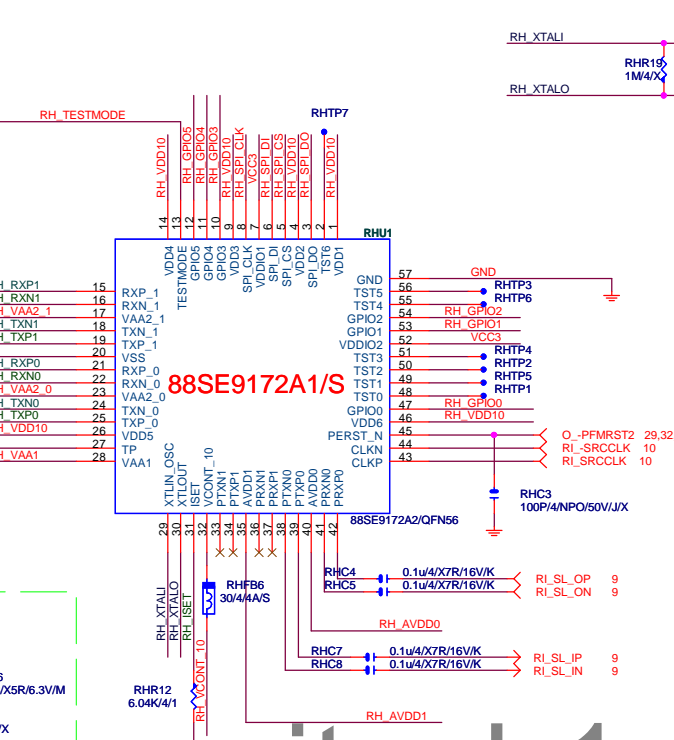
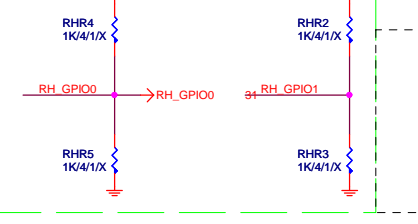
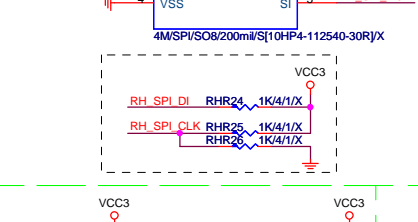
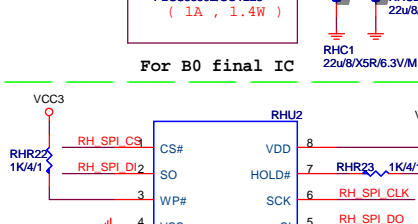
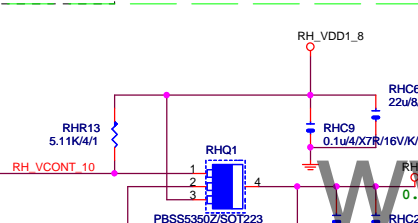
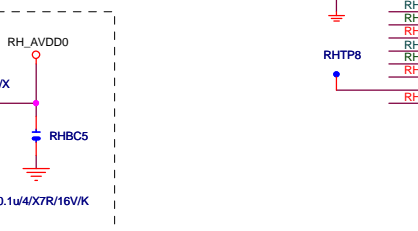
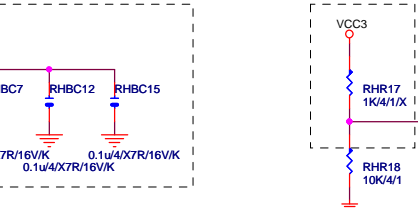
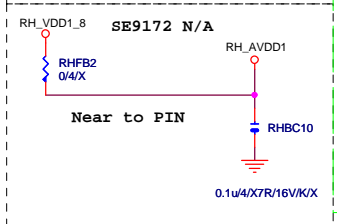
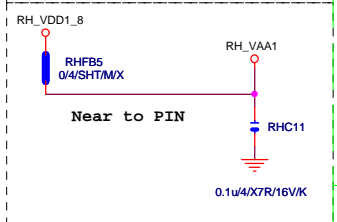
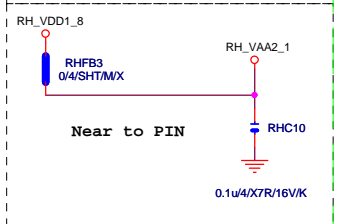
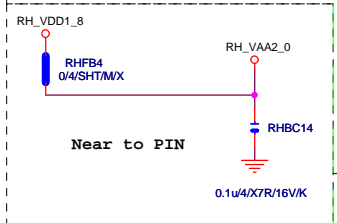
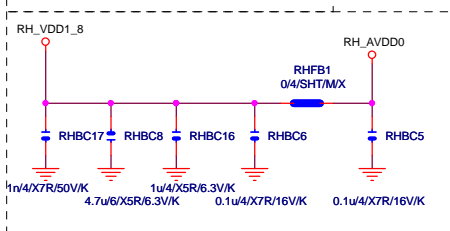
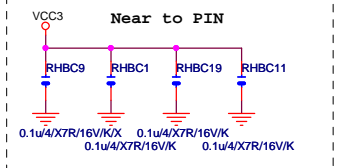
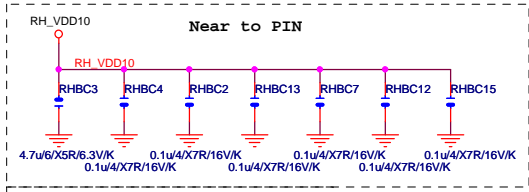
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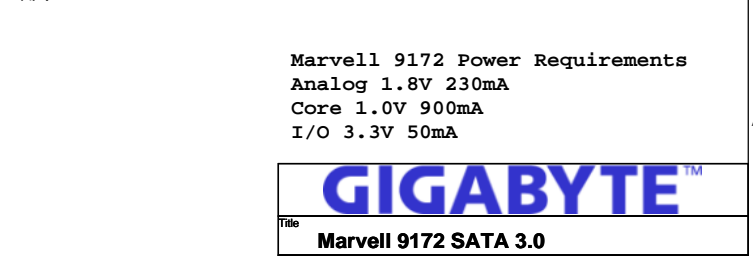
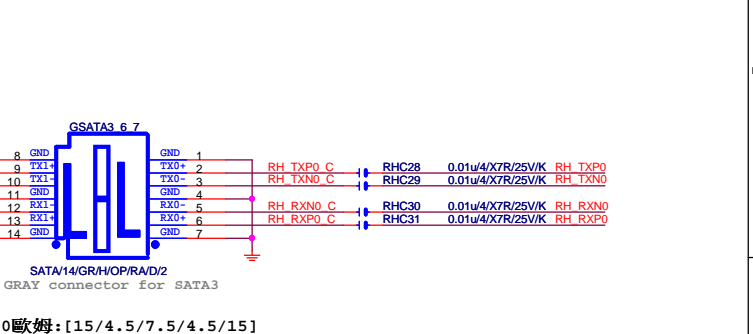
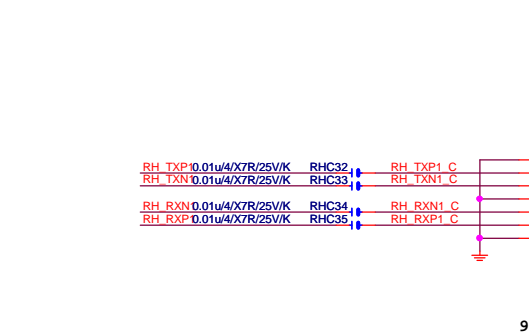
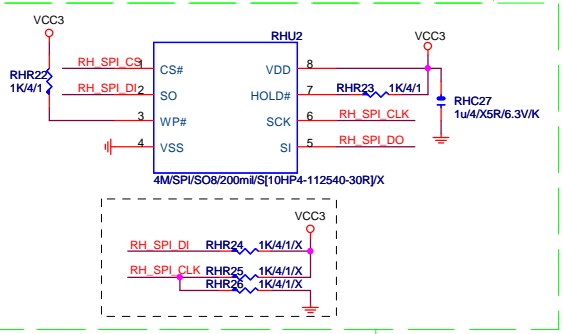
Pin 1 to 6 connection diagram for UESD1. Pin 1 is N_USBP5, Pin 2 is GND, Pin 3 is N_USBP4, Pin 4 is N_USBP4, Pin 5 is FUSEVCC_R6, and Pin 6 is N_USBP5. The diagram shows a bidirectional bus structure with four diodes per line.

AZC099-04S.R7G/SOT23-6L/100DEF-550099-20R_10TA1-018902-10R



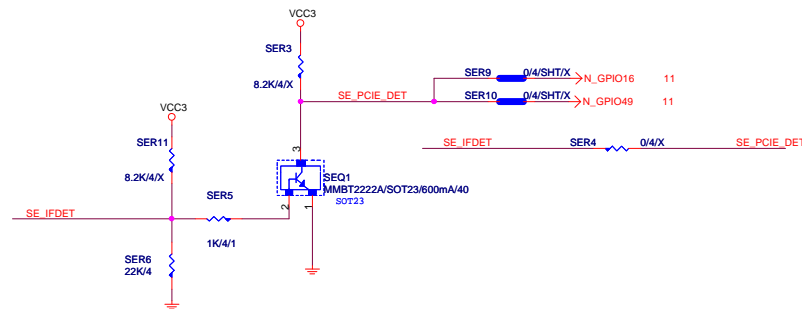
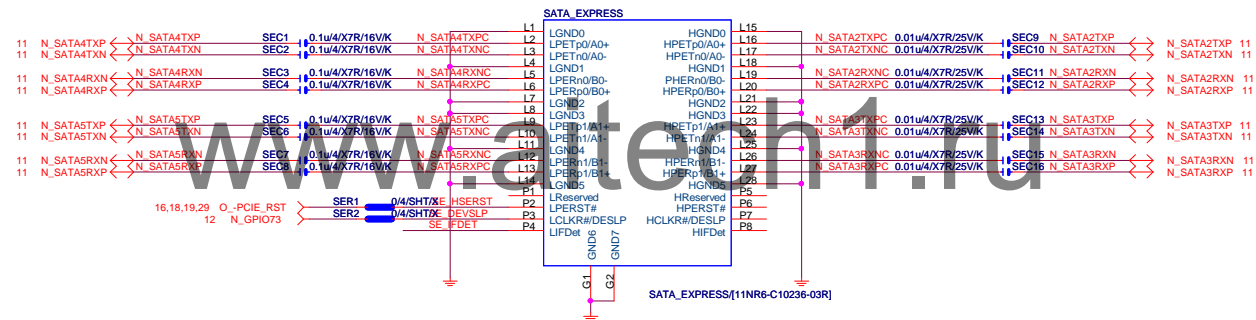


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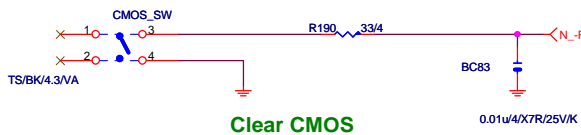
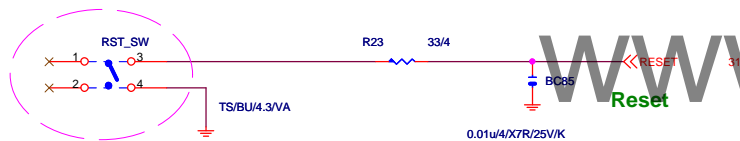
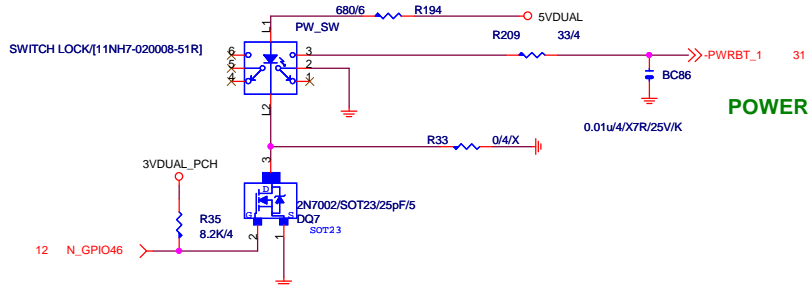
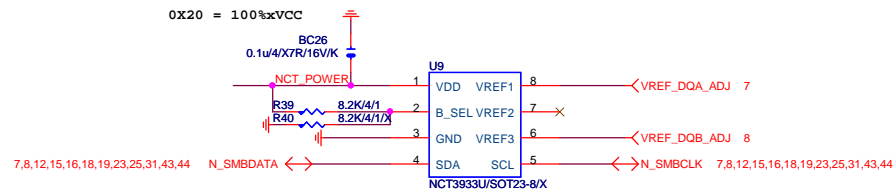
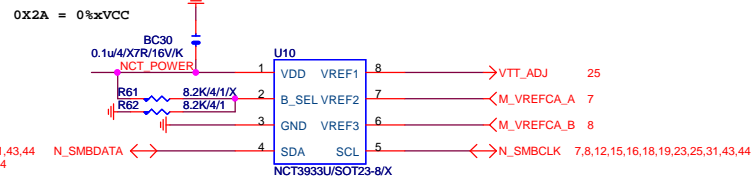
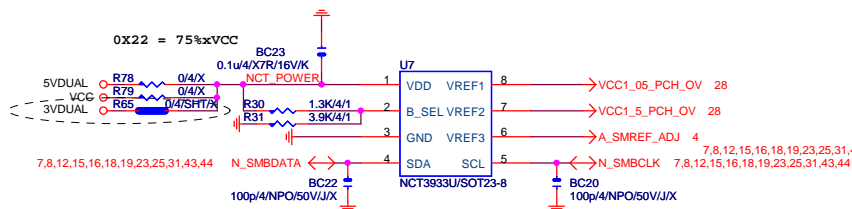


Marvell 9172 Power Requirements
 Analog 1.8V 230mA
 Core 1.0V 900mA
 I/O 3.3V 50mA

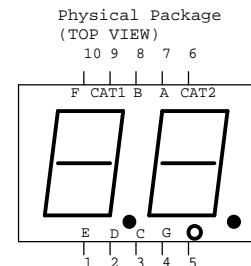
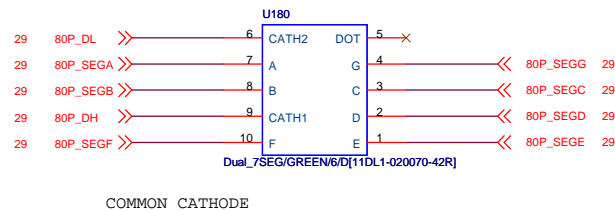
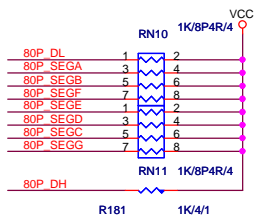
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Size Custom	Document Number GA-Z97X-UD7 TH	Rev 1.0	
Date: Friday, May 09, 2014	Sheet 37	of 49	

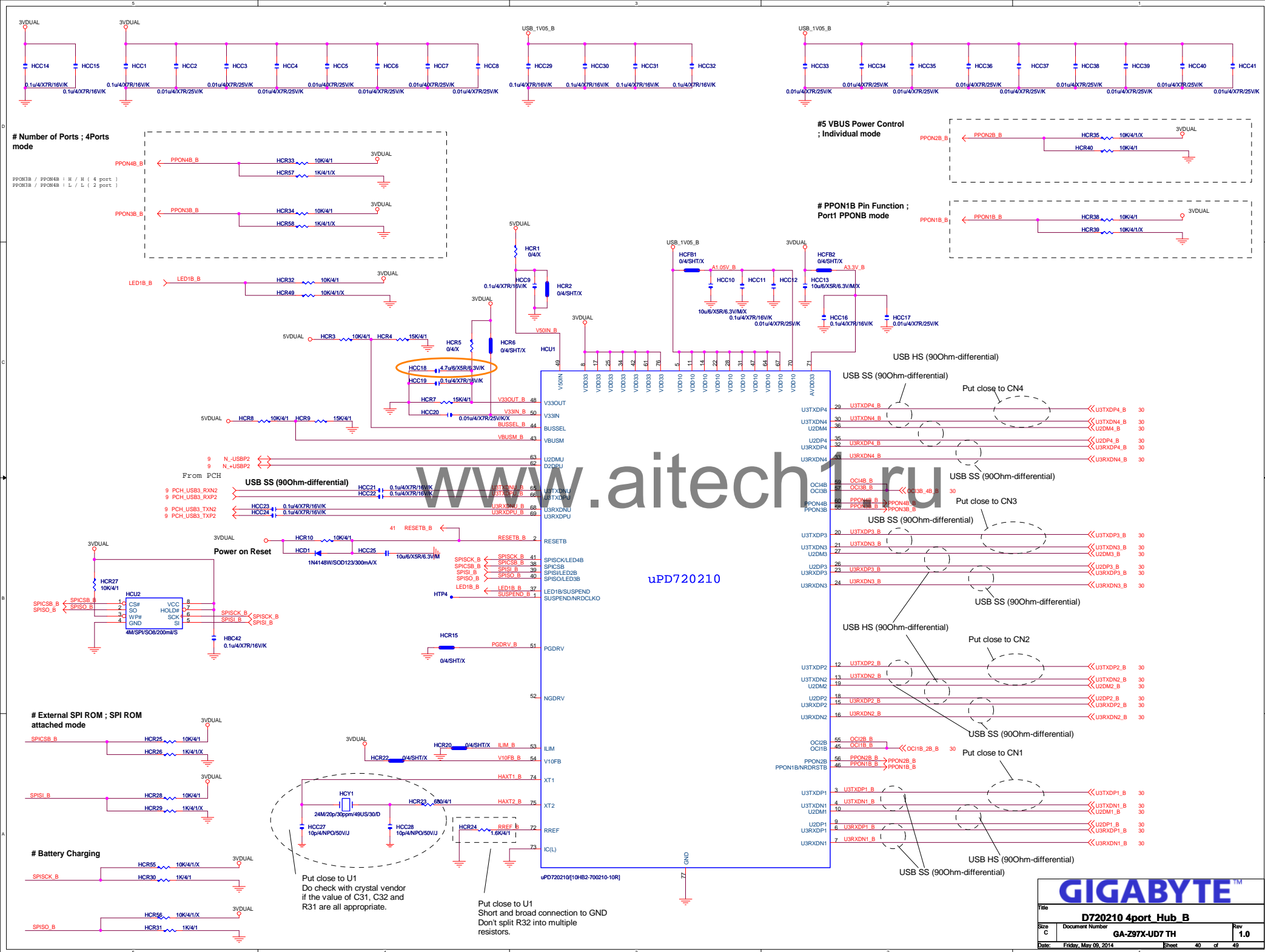


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Size	Document Number	Rev	
Custom	GA-Z97X-UD7 TH	1.0	
Date:	Friday, May 09, 2014	Sheet	38 of 49

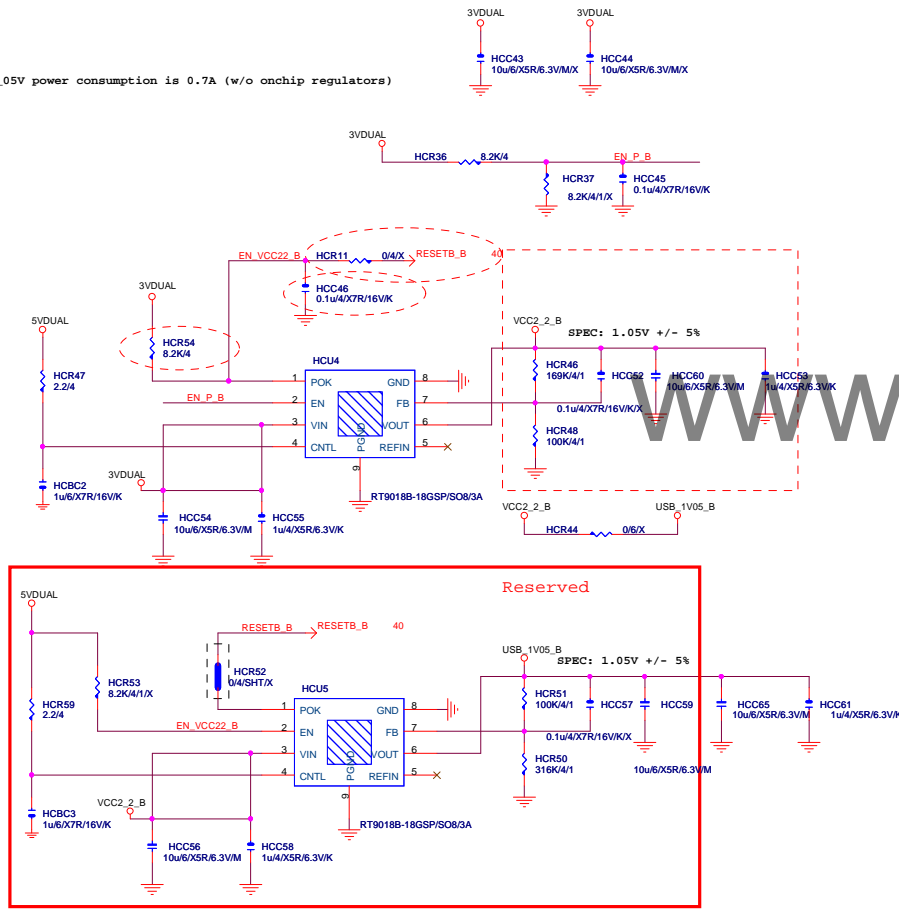


80 PORT



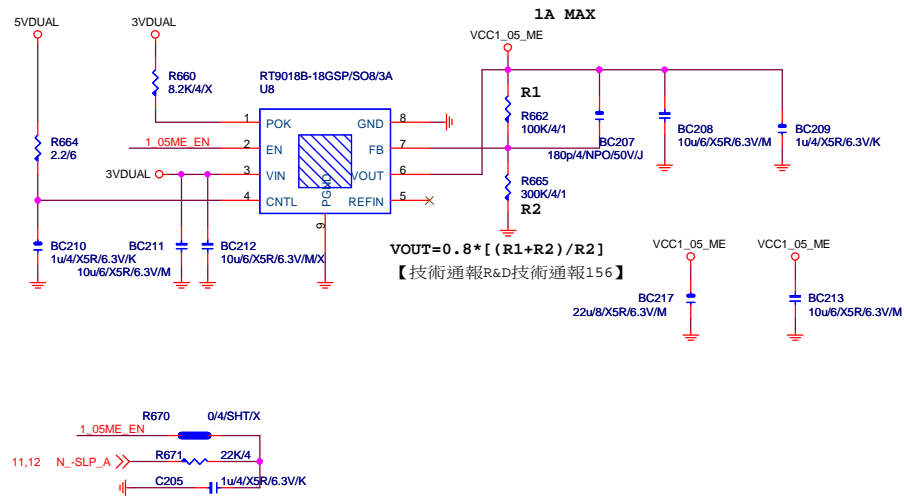


USB1_05V power consumption is 0.7A (w/o onchip regulators)

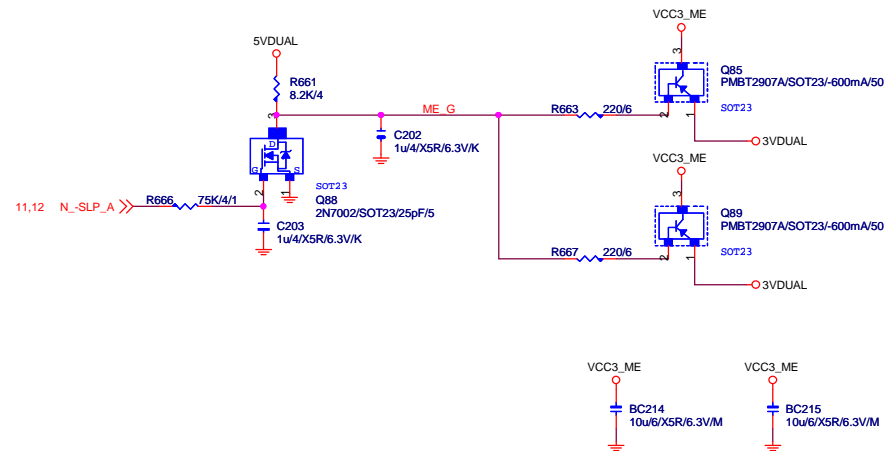


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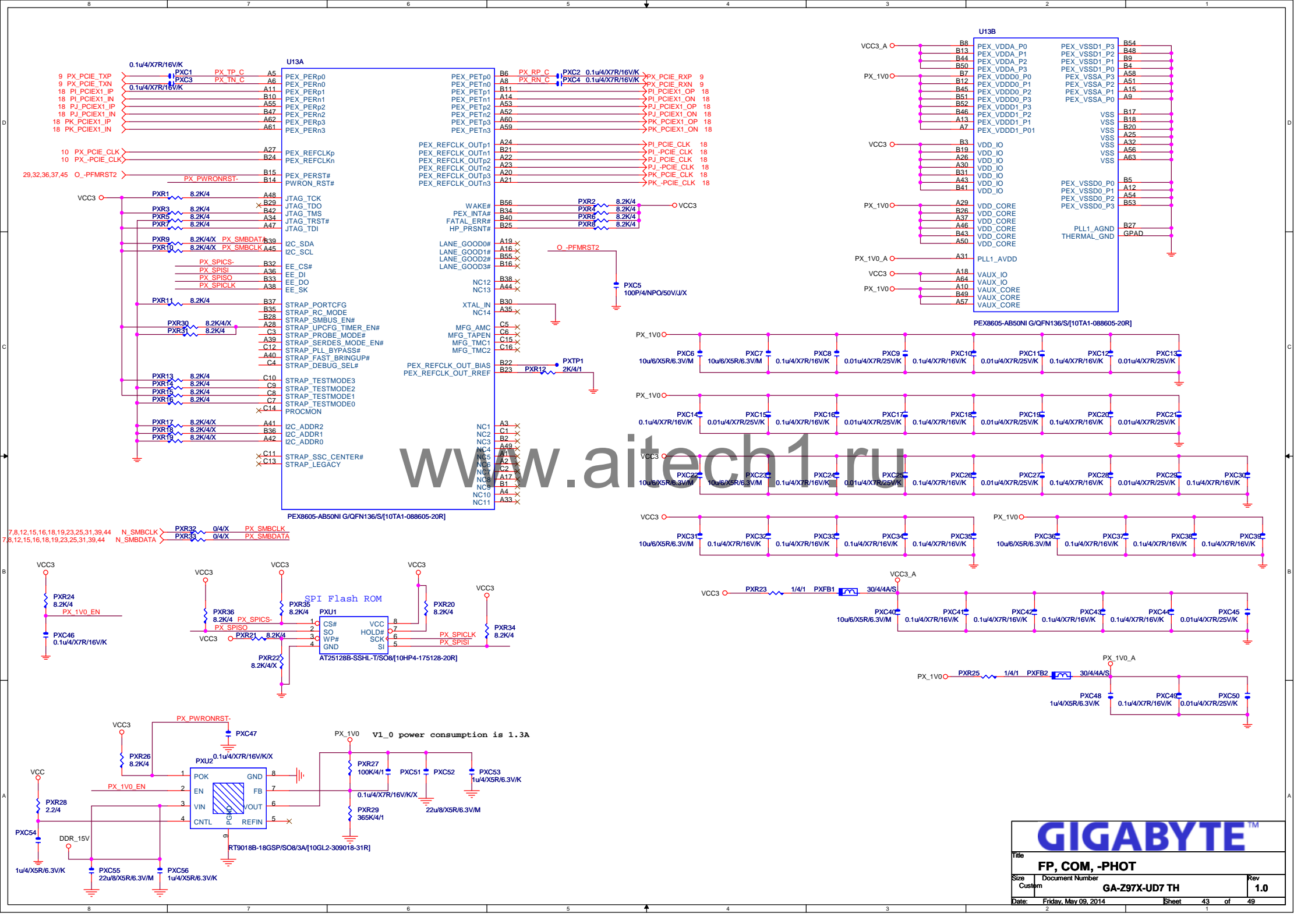
【技術通報R&D技術通報156】
(RICHTER), (NUVOTON), (EMC) 做共用
PIN7分壓阻值須做修改為100K以上電阻值

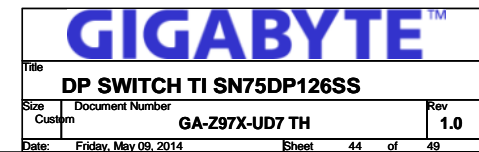
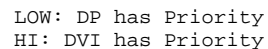
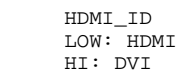


VCC3_ME

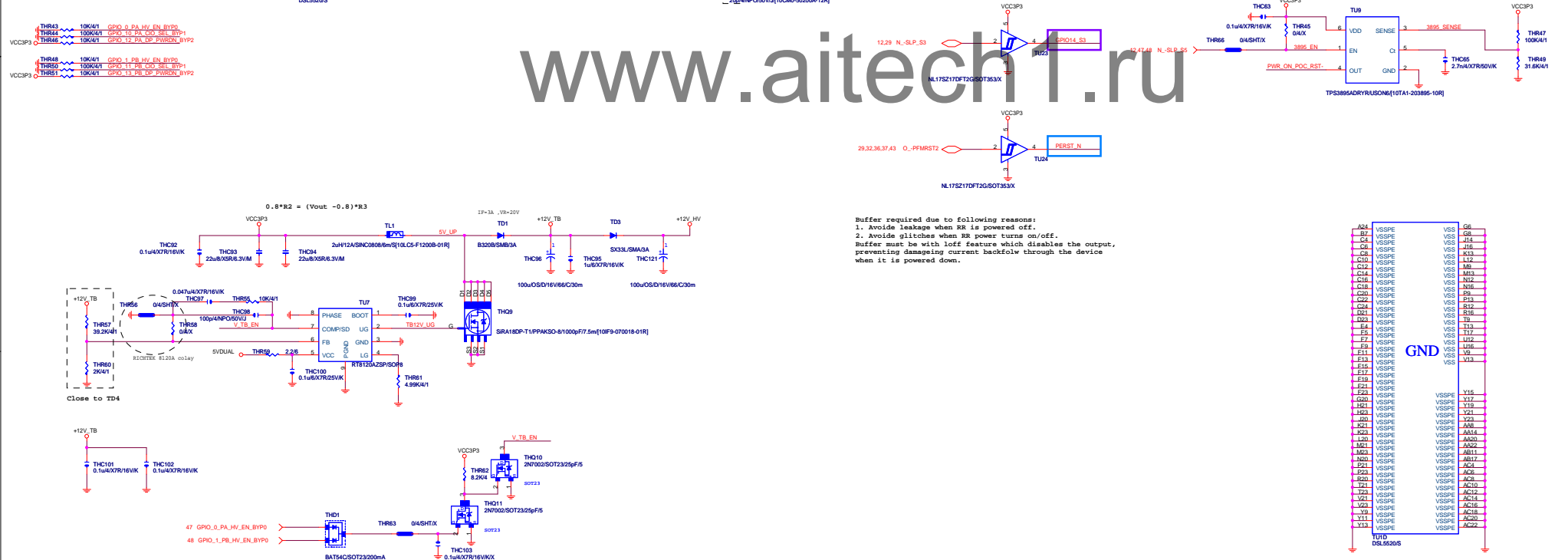
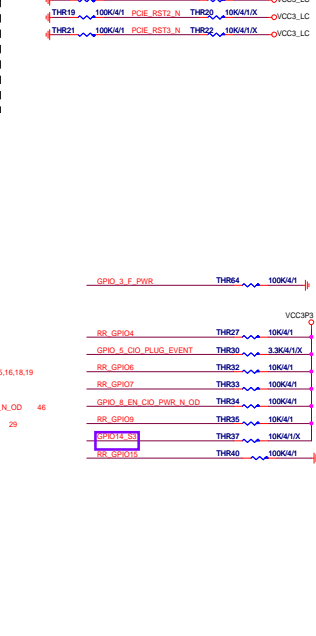
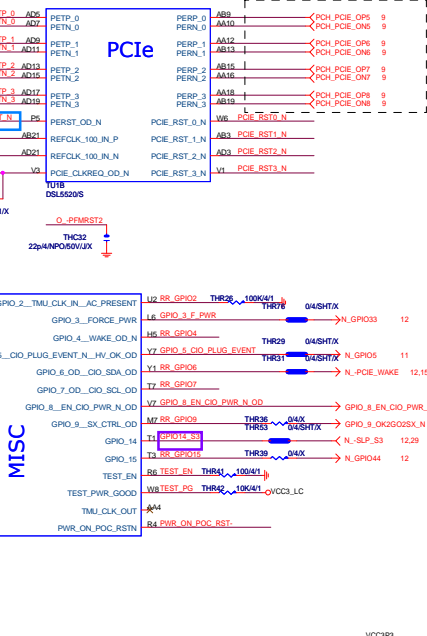
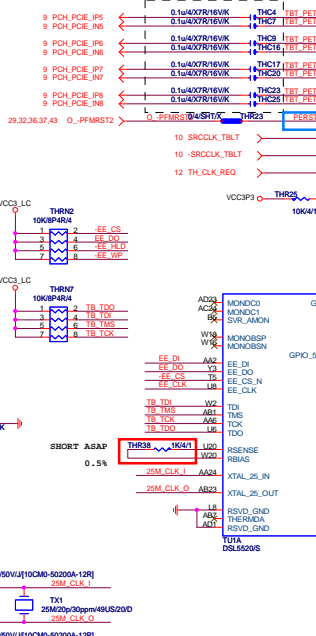
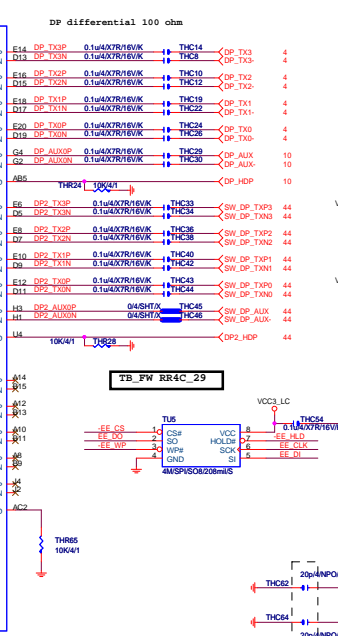


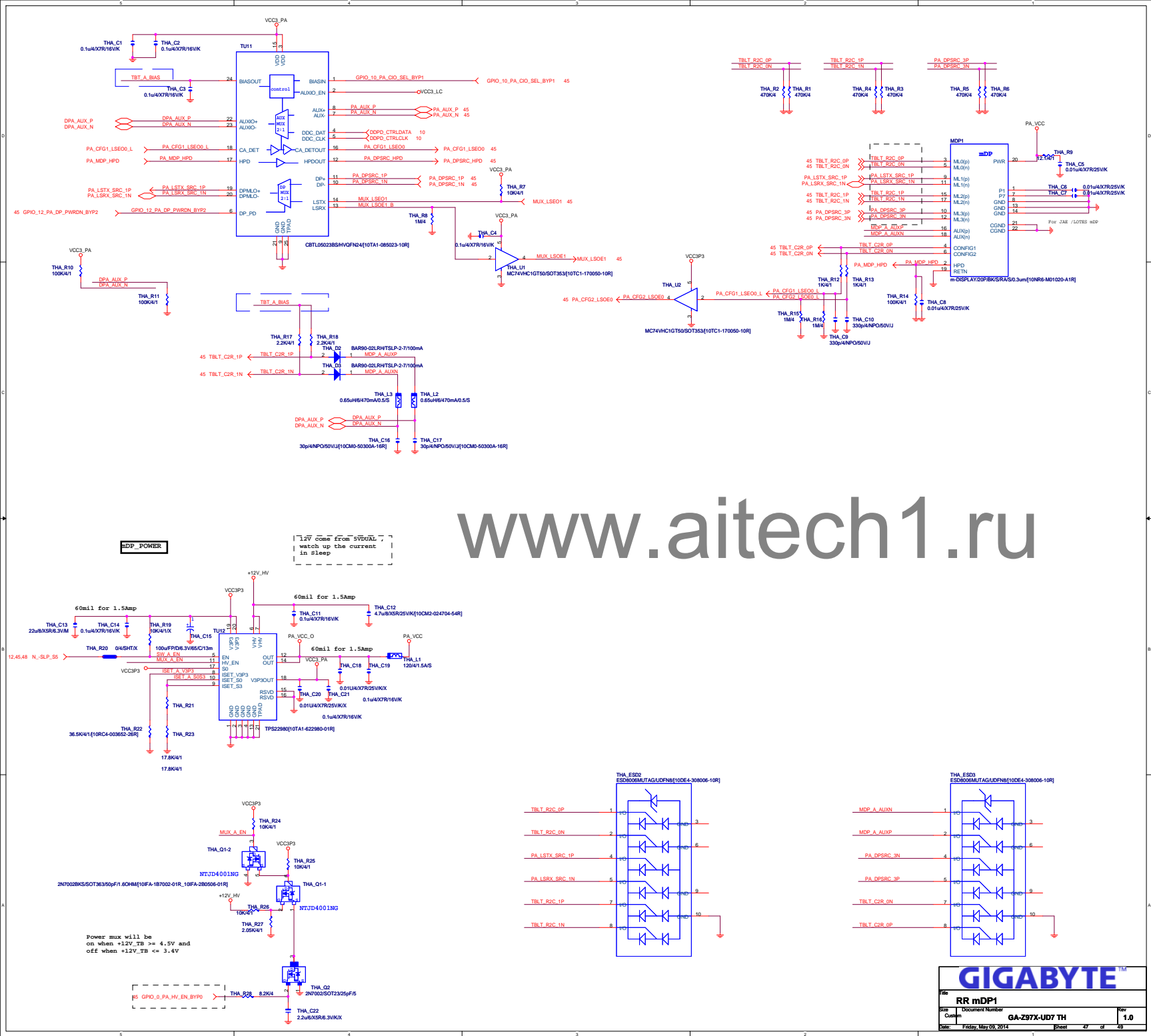
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UIUE	CIO	DP
	PA.DSPRC_3.P	DSPNKO_3.F
	PA.DSPRC_3.N	DSPNKO_3.N
	PA.DSPRC_1.P	DSPNKO_2.F
	PA.DSPRC_1.N	DSPNKO_2.N
	PA.AUX_P	DSPNKO_1.F
	PA.AUX_N	DSPNKO_1.N
	PA.DSPRC.HPD	
	PA.CIO_QX_TP_DP.DSPRC_0.P	
	PA.CIO_QX_TP_DP.DSPRC_2.N	
	PA.CIO_RX_P	
	PA.CIO_RX_N	
	PA.CONFIG1_CIO_0.LISEO	
	PA.CONFIG2_CIO_0.LISEO	
	PA.CIO_QX_TP_DP.DSPRC_2.P	
	PA.CIO_QX_TP_DP.DSPRC_2.N	
	PA.CIO_RX_P	
	PA.CIO_RX_N	
	PA.LSTX_CIO_3.LISEO	
	PA.LSRX_CIO_3.LISEO	
	GPID_0_PA.HV.EN_BYPO	
	GPID_10_PA.CIO_SEL_BYPI	
	GPID_12_PA_DP.PARDEN_BYPI2	
	PB.DSPRC_3.P	
	PB.DSPRC_3.N	
	PB.DSPRC_1.P	
	PB.DSPRC_1.N	
	PB.AUX_P	
	PB.AUX_N	
	PB.DSPRC.HPD	
	PB.QOZ_TX_TP_DP.DSPRC_0.P	
	PB.QOZ_TX_TP_DP.DSPRC_0.N	
	PB.QOZ_RX_P	
	PB.QOZ_RX_N	
	PB.CONFIG1_CIO_2.LISEO	
	PB.CONFIG2_CIO_2.LISEO	
	PB.CIO_QX_TP_DP.DSPRC_2.P	
	PB.CIO_QX_TP_DP.DSPRC_2.N	
	PB.CIO_RX_P	
	PB.CIO_RX_N	
	PB.LSTX_CIO_3.LISEO	
	PB.LSRX_CIO_3.LISEO	
	GPID_1_PB.HV.EN_BYPO	
	GPID_11_PB_CIO_SEL_BYPI	
	GPID_13_PB_DP.PARDEN_BYPI2	
		DSPNKO_3.F
		DSPNKO_3.N
		DSPNKO_2.F
		DSPNKO_2.N
		DSPNKO_1.F
		DSPNKO_1.N
		DSPNKO.AUX.F
		DSPNKO.AUX.N
		DSPNKO.HPD
		DSPNKO_3.F
		DSPNKO_3.N
		DSPNKO_2.F
		DSPNKO_2.N
		DSPNKO_1.F
		DSPNKO_1.N
		DSPNKO.AUX.F
		DSPNKO.AUX.N
		DSPNKO.HPD
		DSPNKO_3.F
		DSPNKO_3.N
		DSPNKO_2.F
		DSPNKO_2.N
		DSPNKO_1.F
		DSPNKO_1.N
		DSPNKO.AUX.F
		DSPNKO.AUX.N
		DSPNKO.HPD





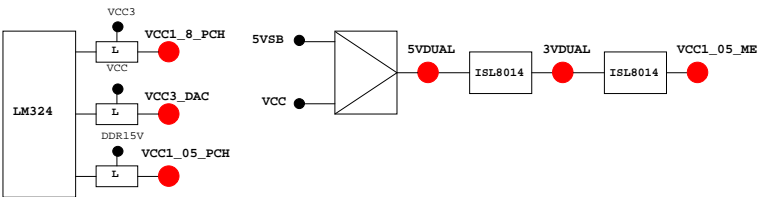
PCB GPIO LIST TABLE

PIN NAME	PWR	AFTER PLTFRST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SEN	LOW_PWR_1	
VIDO5/GP27/SEN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CsISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



散熱模組料號:

BIOS超電壓對應表:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_AVREF_CA_B	DRAM Address Ref
VREF_DQ_AVREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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TABLE LIST			
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